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Circuit Diagram AI 016856 E
PCB Assembly AH 016856 E

1 General description

The eight Soleniod Driver outputs can be arranged as pull-up outputs (to a common + supply) or as pull-down outputs (to a common - supply) The outputs are protected against overvoltage or wrong polarity of the supply overcurrent and are isolated from system potentials but not from one another

Eight digital inputs are also available in the module. They are isolated from system potentials but not from one another

The Solenoid Driver module communicates with the FICS-11 Main Controller via the serial DECA bus link on the back ribbon cable for both the outputs and inputs. The output circuitry requires two blocks of data via the DECA bus; one for the output pattern and one for the module address.
The digital inputs are requested when required by the Main Controller sending an address plus a read signal. The digital inputs are then clocked out at the Solenoid Driver module to the Main Controller.

The 5V and 24V voltages and the maximum time allowed between communications transactions are monitored. The outputs are switched off if a fault is detected.

2 Description of circuit elements

Refer to ciruit diagramm AI 016856E and PCB assembly AH 016856E.

Refer to the description of the Main Controller for full details of DECA bus transactions.

2.1 Module addressing and read/write decoding)

The circuitry associated with the module addressing is shown on sheet 1.

The serial data from the DECA bus is clocked into the shift registers U2-C, U2-B and U8-B. The 7 bit address is contained in the Q0 to Q3 outputs of U2-B and Q1 to Q3 outputs of U2-C. These are compared with the back plate switches connected to the second inputs of U3-B, C, D and E and U5 - B, C and D. The result of this comparison is fed to U7-C pin 9 and a valid address condition will be clocked to the D-type flip flop U7-C pin 13 Q output by the DECA strobe pulse to U7-C pin 10. The U7 pin 13 Q output is fed to both AND gates U6-B and U6-E.

The read/write line from the shift register U2-C Q0 output pin 13 is inverted by U5-E and fed to the D input of U7-B. The DECA strobe pulse to U7-B pin 3 clocks the read or write condition to the input of dual input AND gate U6-E pin 2.

A "high" at U6-E pin 3 output provides a write strobe signal to the shift and store register U8-B thus allowing the data in the input registers of U8-B to be transferred to its output storgage registers.

A read signal is produced at the output of U6-E pin 11 by ANDing the valid address signal and the inverse (not Q) output of U7 pin 2. The read signal enables the DECA bus data driver U10-B and at the same time puts the shift register U11-B into serial out mode via inverter U13-B.

2.2 Isolated supplies for the outputs and output drivers.

The incoming supply is derived from an external source and is not connected to system potentials within the module. The supply is protected from over current with a 10Amp. fuse, FS1, fitted internally.

2.2.1 Standard pull-up version

The incoming positive wire is connected to rear terminals 15 and 16 and the negative wire to terminals 13 and 14. The supply is connected to all the output stages. The circuitry for the driver supply for the opto-isolators and for overvoltage protection is shown on sheet 1.

For the standard pull-up version the components fitted are as shown exept that D6A, D7A and D8A are not fitted.

Overvoltage is sensed by zener diode Z8 which conducts at voltages exceeding about 56V. Overvoltage causes Q7 to switch on which then triggers Q8 on, causing a short circuit of the supply and hence a rupture of fuse FS1. A spare fuse is fitted on the P.C.B.

A -3,3V voltage with respect to the common positive rail for the opto-isolators and drive transistors on the output side is derived from the external negative rail with components Q3, Q4, Q5, D6, R27, R22 , R23 and R28. Q5 is controls the voltage across R28 via the negative feedback of its collector to the bases of Q3 and Q4. The total current drawn through Q3 and Q4 collectors is largely independennt of the external supply voltage.

2.2.2 Optional pull-down version

The incoming negative wire is connected to rear terminals 15 and 16 and the positive wire to terminals 13 and 14.

Overvoltage protection works in the same way as the standard pull-up version exept that D7A and D8A are fitted instead of D7, D8. and that Q7 becomes a PNP transistor; i.e. the circuit works as before except in the opposite polarity.

Similary a +3,3V voltage for the isolators and drive transistors of the output is derived with repect to the common negative rail. Here D6A is fitted instead of D6 and Q3, Q4 and Q5 are PNP transistors.

2.3 Solenoid Driver outputs

Except for the higher output rating of channel 8, where there is a 2A maximum instead of a 1A maximum for channels 1 to 7, all channels are identical.
A full description will be given for channel 1 only.

2.3.1 Standard pull-up version

Pull-up outputs have a common positive connection, the positive potential of the external supply. The outputs shown on sheet 3 are drawn for the standard pull-up version. Channel 1 comprises U24-B, U26, U34, Q17, Q25, Q33 and associated resistors and links. For this version links 23, 55, 31 and 63 are fitted and D41 is fitted. Links 7, 39, 15 and 47 are not fitted and D41A is not fitted.

To switch an output on, the high going digital drive signal at U24-B pin 2 causes the output at pin 3 to go low providng the Q0 output of U22-B pin 13 (derived from the monitor circuit inputs to U22-B) is high. A low signal from U24-B pin 3 will cause U26 opto-isolator output transistor to switch on causing Q17 and the output transistor Q25 to switch on also. The output transistor is therefore pulled up to the positive supply rail (or very nearly) and is protected against switching transients by D41.

The output current passing through R104 is normaly low enough to prevent Q33 from switching on. When the current exceeds about 1A the voltage developed across R104 will cause Q33 to switch on. The current detect signal at U34 output transistor, which is normally pulled high by R72, will be pulled low for an over- current condition.

Note:
The 2A trip level in channel 8 (only) is achieved by using two resistors R111 and R136 in parallel. The trip point is therefore twice as high as other channels.

2.3.2 Optional pull-down version

Pull down outputs have a common negative connection, the negative potential of the external supply to rear terminals 15 and 16.

For the pull-down version Q17 and Q33 become NPN transistors and Q25 becomes a PNP transistor. In addition links 7, 39, 15 and 47 are fitted and D41A is fitted. Links 23, 55, 31 and 63 are not fitted and D41 is not fitted.

As for the pull-up version the digital drive signal causes output transistor of U26 to switch on provided the monitoring circuits through U22-B allows this. The switching actions remain the same as for the pull-up version except that the polarities are reversed. Here the emitter of Q25 switches to the common regative (or very nearly).

Over-current detection through R104, Q33 and U34 is the same as the pull-up version except that the polarity is reversed.

2.4 Monitor circuit

2.4.1 5V supply

The 5V supply is monitored by R14, R15, D4 and Q1as shown on sheet 1. Q1 will be switched on providing the 5V supply is above approximately 4.5V.

2.4.2 Module address

Q2 will be switched on if the module is regularly being addressed and the 5V through Q1 is present. The output of monostable U12-C at pin 10 will be kept high provided it receives trigger pulses from U13-B pin 3, i.e. from U6-E pin 11 which regularly toggles after an address acknowledge for digital input reads. Digital inputs are read every 20 msec. and the time out period of U12-C is about 56msec. The output of U-13 pin 10 will switch high, thus switching off Q2, if the time out preriod is exceeded.

When Q2 switches off the supply for the opto isolators driving the outputs is removed and the outputs are therefore all switched off. At the same time the low going output from U12-C (output clear signal to diodes D33 to D40) will force the Q0 to Q3 outputs of U22-B and U23-B quard catches to switch off, thus also switching all outputs off.

D5 is the green front facia LED indicating that the module is addressed and that the 5V suppply is present. R13 and C2 provide a short delay of about 0.5 sec. after power-up to the enable pin 13 of U12-C and the second input of the NAND gate U13-D. This ensures that there are no transient switchings of the outputs. On power-down D3 rapidly discharges C2 so that the same delay is ensured with every power-up.

2.4.3 Overcurrent trip

Each output has its own current detection mechanism already described described above. The current detect signals generated in the opto-isolators of the output stages are connected to their respective reset inputs R0 to R33 on U22-B and U23-B. An over current in an output stage causes the respective current detect signal to go low causing the corresponding latched Q output from U22-B or U23-B to switch off. The Q output switching off causes the output itself to be switched off and therefore returning the current detect signal to high. The output will remain switched off however until a pulse through C4 from the current trip oscillator comprising U13-C, R19 and C3 causes the Q output to switch on again. This trip-and-try- again action with a period of about 1.5sec will continue until the current drawn from the output is less than the over current detect level.

2.5. Digital Inputs

All the digital inputs are identical and are shown on sheet 2. Only channel 1 will be described.

The channel 1 input consists of a rectification diode D9 and a constant current source consisting of Q9, R32, R40, D17 and D18 which supplies the opto-isolator U14. The output of U14 is smoothed by R48 and C21. The logic level at the junction R48 and R56 is read by the shift register U11 (sheet 1) Normally the p/s line on U1 is high, keeping the shift register in the parallel mode. When the Main Controller requests a read the shift register is put into the shift mode and the bus transmitter U18 is enabled. The Main Controller clocks the data out of U1 through the D-type flip-flop U9-C and to the DECA bus via the transmitter U10-B.

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Appendices:

Circuit diagram	AI 017827 F
PCB assembly	AH017827 F

1 General description

The Relay Output module provides eight separate single pole change over contacts for driving external devices such as contactors. The outputs are isolated from one another and from system potentials.

The module communicates with the Main Controller via the DECA bus on the back ribbon cable. The Main Controller sends two blocks of data, an address block and a block containing the output information. If the address coincides with the module address the output block data is accepted and used to drive the outputs accordingly.

The 5V and 24V voltages and the maximum time allowed between communications transactions are monitored. The outputs are switched off if a fault is detected.

2 Description of circuit elements

Refer to circuit diagram AI017827 and PCB Assembly AH017827.

Refer to the Main Controller description for full details about DECA bus communication transactions.

Note that in this description integrated circuits have been identified with the prefix "U--", as standard practice, although the prefixes in the circuit diagram here are "IC--". The circuit diagram will be changed to "U--" at the next issue.

2.1 Module Addressing

The serial data (via U1 pin 5) from the DECA bus is clocked (via U1 pin 3) into shift registers U2, U3. The seven bit address is contained in U2 and is compared to the module address via U4, U5, U6 and U7. The result of this comparsion (address valid) is routed to the D-type flip-flop data pin 5 of U8. On receipt of the DECA strobe positive edge this result is clocked to the "Q" of the flip-flop U8 pin 1. The "Q" (address coincidence) output will now remain active until reset by the DECA reset.

2.2 Output Update

The read/write signal on U2 pin 5 is inverted by U5 and routed to the D-type flip-flop data pin 9 of U8. The positive edge of the DECA strobe will transfer this read/write signal to the "Q" output of the flip-flop U8 pin 13.

If both the address coicidence and the gated read/write signal are active (high) then the strobe input to shift register U3 pin 1 will go high (TP20). With this strobe input high the data associated with the address decoded will be transfered to the output latches of U3.

Each output of U3 drives a relay via transistors T1 to T8. To reduce contact wear a RC suppression network is provided in paralled to both the normally open and normally closed relay contacts.

2.3 Monitoring

The watchdog circuit monitors the address coincidence pulses and all voltage rails. The circuitry associated with the watchdog consists of monostable U9 whose output (pin 10) is kept high providing the period between address coincidence pulses does not exceed 6 seconds, (worst case output update interval). Should this output drop low, through lack of address coincidence pulses, the outputs of U3 will be set to their tri-state condition by pin 3 of U6 driving the output enable of U3 low and turning off the front panel LED (D1) off via transistor T11. With the outputs of U3 in their tri-state condition the output transistors will be deprived of their base drive currents and will thus turn off.

Transistor T10 together with zener diode Z1 detects the level of the 5 volt rail. Should the 5 volt rail fall below. about 4.6 volts T10 will turn off thus removing the supply voltage for the relays and turning off the front panel LED.

Should the 24 volt rail fail both the output relays and the front panel LED will be deprived of drive voltage.

Components C24, R52 and D10 ensure a controlled output enable after power-on.

Contents

Appendices:

Circuit Diagram	AI 150058 D
PCB Assembly	AH 150058 D

1 General description

The Relay Out/Digital In module provides eight relay contacts for driving external devices (such as contactors) as well as eight digital inputs.

There are eight relay outputs which can be arranged as normally open or normally closed contacts. The first six outputs are isolated from one another whereas the seventh and eighth are connected together with a common connection as not more than 24 rear terminals are available.for customer connections.

All inputs and all outputs are isolated from system potentials and inputs are isolated from outputs.

The module communicates with the Main Controller via the DECA bus on the back ribbon cable.

The 5V and 24V voltages and the maximum time allowed between communications transactions are monitored. The outputs are switched off if a fault is detected.

2 Description of circuit elements

Refer to ciruit diagramm AI 150058 and PCB assembly AH 150058.

2.1 Module addressing and read/write decoding

The circuitry associated with the module addressing is shown on sheet 1.

Refer to the description of the Main Controller for full details about DECA bus transactions.

The serial data from the DECA bus is clocked into the shift registers U2, and U8. The 7 bit address is contained in the Q0 to Q3 outputs of U2-A and the Q1 to Q3 outputs of U2-B. These are compared with the back plate switches connected to the second inputs of U3-A, B, C and D and U5 - A, B and C. The result of this comparison is fed to U7-B pin 9 and a valid address condition will be clocked to pin 13 Q output by the DECA strobe pulse to pin 10. The U7 pin 13 Q output is fed to both AND gates U6-A and U6-D.

The read/write line from the shift register U2-B Q0 output pin 13 is inverted by U5-D and fed to the D input of U7-A. The DECA strobe pulse to U7-A pin 3 clocks the read or write condition to the input of dual input AND gate U6-A pin 2.

A "high" at U6-A pin 3 output provides a write strobe signal to the shift and store register U8 thus allowing the data in the input registers of U8 to be transferred to its output storage registers.

A read signal is produced at the output of U6-D pin 11. by the ANDing of the valid address signal and the inverse (not Q) output of U7-A pin 2. The read signal enables the DECA bus data driver U10-A and at the same time puts the shift register U11 into serial out mode via inverter U13-A.

2.2 Relay Outputs

An address co-incidence and a write signal allow the data associated with the address to be transfered to the output latches of U8 which in turn drive the individual darlington buffers in U14.

Each output of U14 drives a relay coil as shown on sheet 3. To reduce contact wear an RC suppression network is provided in paralled to both the normally open and normally closed relay contacts.

2.3 Monitor circuit

2.3 1 5V supply

The 5V supply is monitored by R16 R17, D5 and Q2. Q2 will be switched on providing the 5V supply is above approximately 4.5V. With Q2 switched on the +24V is switched through as a common positive supply for the relay coils.

2.3.2 Module address

The output of monostable U12-B at pin 10 will be kept high provided it receives trigger pulses from U13-A pin 3, i.e. from the device which regularly toggles after an address acknowledge for digital input reads. Q1 will therefore be switched on if the module is regularly being addressed and the 5V supply is present. Digital inputs are read every 20 msec. and the time out period of U12-B is about 56 msec. The output of U-13 pin 11 will switch low thus dis-enabling U8 and the drive to the output buffers if the address monitor time out period is exceeded.

D4 is the green front facia LED and is illuminated when the module is addressed and that the 5V supply is present. R11 and C2 provide a short delay of about 0.5 sec. after power-up to the enable pin 13 of U12-B and the second input of the NAND gate U13-C. This ensures that there are no transient switchings of the outputs. On power-down D3 rapidly discharges C2 so that the same delay is ensured with every power-up.

2.4. Digital Inputs

All the digital inputs are identical and are shown on sheet 3. Only channel 1 will be described.

The channel 1 input consists of a rectification diode D7 and a constant current source consisting of Q4, R20, R28, D15 and D16 which supplies the opto-isolator U15. The output of U15 is smoothed by R36 and C17. The logic level at the junction R36 and R44 is read by the shift register U11 (sheet 1)

Normally the p/s line on U1 is high, keeping the shift register in the parallel mode. When the Main Controller requests a read the shift register is put into the shift mode and the bus transmitter U10-A is enabled. The Main Controller clocks the data out of U11 through the D-type flip-flop U9-A and -B and to the DECA bus via the transmitter U10-B.