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1 General description

One Analogue Acquisition Module provides the capability to connect up to sixteen separate analogue inputs to the FICS-11 system. The negative wires of all inputs are connected together and to system 0V. The module provides all the necessary analogue to digital conversion and input linearisation.

Once the module is powered-up correctly, it will select and read the first input channel and then wait until it receives a single data byte on the "M" bus that matches the modules address. Once the address has been received and verified the Analogue Acquisition module transmits five data bytes: the first is the channel number (0-15) and the following four bytes contain the latest value of that channel. The module then proceeds to select and read the next channel in preparation for the next poll (module address).

To maintain the accuracy of conversion a zero reference measurement is taken after each of the sixteen input channels has been sampled. This reference measurement is than used as an auto-zero correction for the next sixteen readings.

The module is designed around a microprocessor and the module includes both RAM and EPROM memory. One EPROM contains the module firmware and the other the customer specific input defintion, i.e. input type, range and linearising for the various types of inputs which can be connected to the input terminals.

Analogue inputs may be either 0...10V (standard) or 0-1V (non-standard) and represent 0...100% of rangee of the input defined for their respective channels. Fail safe checks are incorporated into the hardware and software. Faulty module addressing or software watchdogging will cause the front green LED to flash instead of illuminating constantly as it does when the module is working correctly.

Reading Validity - each auto zero reading is checked. If the detected value is below a certain level the module is deemed to have failed. In such an event the last verified value for each of the inputs is returned until the auto-zero reading is again correct.

Note:
A single FICS-11 system can support up to sixteen control loops (internal or external). Each of the control loops in a system must have at least one analogue input associated with it. All analogue inputs used for loops, (and any additional analogue inputs used as alternatives to any of the control loops), must be sited on the first analogue acquisition module in a system containing two or three modules. The second and third modules are available for monitor inputs only.

Analogue inputs used for control loops have a maximum waiting time, guaranteed by the Main Controller, of 340msec between updates.

The update times for non loop inputs when more than one Analogue Acquisition module is fitted is configuration dependent. See the FICS-11 Programmer`s Manual for further details.

2. Description of circuit elements

Refer to circuit diagram AI016616 and PCB assembly AH016616

Refer to the Main Controller description for full details about DECA bus communication transactions.

Note that in this description integrated circuits have been identified with the prefix "U--", as standard practice, although the prefixes in the circuit diagram here are "IC--". The circuit diagram will be changed to "U--" at the next issue.

2.1 Address Decoding

All address lines are un-buffered and are driven directly from the 6809 (IC17). Basic decoding is performed by multiplexer IC21. This provides all the enable signals through the various links (see Table 1.1) to the memory sites PROM 1 (IC22), PROM 2 (IC23), RAM1 (IC19), the 6850 VIA (IC29) and via a further decoder IC13 to the Hex D-type flip-flops (IC1, IC2, IC3, IC4) and the module address reader IC14.

Data control is achieved in the individual devices, apart from the module address switch which is read through tri-state buffer IC14, and the data to the D-type flip-flops is inverted by the Hex Inverter IC10.

2.2 Watchdog

The module will reset itself with a hardware watchdog if the software does not confirm its operational status within a specified time, nominally set at 250 milli-seconds. This may be caused by a communications failure, an input conversion failure of the Auto-Zero or of one of the inputs.

The hardware system watchdog is based on a retriggerable monostable built around op-amp IC30. This device with its associated components C30 and R68 forming the time interval while R65, R66, R67 define the switch threshold.

Providing that C30 is continually discharged by transistor T3 (via current limit R64) the negative input of IC30 pin 3 and the output of IC30 pin 7 will remain high. With the output of IC30 pin 7 high the system reset, IC17 pin 37, will not be active and the red LED 1(fitted internally) will remain off. The base of T3 is driven by the input sample and hold gate control from IC7 pin 11 via C29 and R63. R80 ensures that T3 is normally held off.

The green LED2 (on the front facia) is used to confirm that the module is being addressed an that there is no watchdog.. It is driven by transistor T6 which in-turn is controlled by the voltage appearing across C61. Capacitor C61 forms the default timeout interval with R74 and R75. The actual voltage level is held under control by transistor T5 continually holding the charge across C61. Transistor T5 is regularly pulsed by a differentiated input sample and hold control signal. Thus providing the module maintains its input sampling rate the reset will be inactive and the front panel led will remain illuminated.

2.3 Clock Circuits

There are two clocks contained within the module.

a) the 6809 (IC17) module clock, a single 4.000Mhz crystal connected directly across the device and

b) the baud rate clock, a 4.9152MHz crystal forming an oscillator with IC20. The output of this oscillator (IC20 pin 10) drives the clock input (IC26 pin 3) of dual D-type flip-flops (IC26) which performs a divide by four function before the clock is routed to the input of counter IC27 pin 1. This counter provides the transmitt and receive data rate clocks for the ACIA (Asynchronous Communications Interface Adaptor) IC29 at 153.6 kHz.

2.4 Communications

Communications transactions are passed along the Analogue Acquisition "M" bus which works at RS-422 levels. Transactions are received via line receiver IC31, the output of which IC31 pin 3 is routed directly to the ACIA IC29 pin 2. Transactions are transmitted directly from the ACIA IC29 pin 6 to the level shifter/bus transmitter IC32 pin 1.

Data processing is performed by the software.

Refer to the Main Controller description for details about communications transactions.

2.5 Input Data Control

The sixteen analogue input channels enter the module through a low pass filter (R1-R32, C1-C16), into two "one of eight" multiplexers which are controlled by channel selects E0, E1, E2 and Inhibits A and B. Each of these control signals is driven by the software via flip-flop latches IC3, IC4 and the level shifters IC6, IC7.

The selected channel from the multiplexer is then routed to buffer/amplifier IC11 pin 5. Amplifier IC11 is arranged as either a unity gain buffer or as a times 10 amplifer stage.

Amplification is selected when IC7 pin 13 is high where the gain is controlled by resistors R45 and R46 from the buffer output (IC11 pind 4) and the output is passed through an analogue switch IC 16. This switch together with C24 form a Sample and Hold circuit controlled via latch IC4 pin 2 and level shifter IC7 pin11.

Once the input has been captured at C24 it is presented to the invert input comparator IC12 pin 3 via buffer IC11. The input is converted to its digital value using sucessive approxomation techniques. This requires the D to A (IC5 and IC11 pin 12) to provide the second input to the comparator (IC12 pin 2). The comparison is controlled by software via latches IC1, IC2 into D to A IC5 pins 4 to 15. The result of the comparision is montored by IC14 pin 3.

A reference voltage is provided for the D to A converter at IC5 pin 17. This is derived from the precision zener diode Z1, trimmable buffer IC33 and other components to produce an adjustable stable reference at IC33 pin 7.

The selected analogue input value is offset by approximately +440 milli-Volts before conversion. (i.e. prior to the analogue switch IC16 pin 4). This enables the input to be at a measurable zero reading. Also injected at this point is "noise"at a controlled one of four levels. This"noise" is controlled by Noise (LSB) and Noise (MSB) from latches IC4 pin 7 (TP36), IC4 pin 10 (TPT37), via summing amplifier and buffer IC15 and transistor T1. This technique allows a running average filter executed in software to expand the converted 12 bits into an effective 14 bit resolution.

After each 16 input scans a zero reference measurment is taken by shorting the sampled input line with analogue switch IC16 pins 8 to 9 controlled by flip-flop latch IC3 pin 2 via level shifter IC6.

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1 General description

The analogue output moduel communicates with the FICS 10 system via the serial DECA bus for both digital inputs and analogue outputs. Output circuitry requires four blocks of data from the DECA bus. These are: one block for the output channel address,two blocks for the output data and one for the module address.

The output channels consist of sample and hold circuits which are refreshed approximately every 2.2 milli-seconds from the values held in RAM.

The digital inputs are read when required by the Main Controller. This is achieved by the Main Controller sending the module address. the Main Controller will then set the read/write line to read upon which Main Controller will then clock the data out of the module by pulsing the clock line.

2 Description of circuit elements

Refer to circuit diagram AI 016616 G and PCB assembley AH 016616 F.

Refer to the description of the Main Controller for full details about DECA bus transactions.

2.1 Module Addressing and Read/Write Decoding

The circuitry associated with module addressing is shown on sheets 1 and 2 of the circuit diagram. The serial data from the DECA bus is clocked into the shift register U4-U7 via bus receiver U1 (sheet 1). The seven bit address is contained in U4 and is compared with the module address switches by U2, U3, U8 and U9.The result of this comparison (val add) is fed to the D-type flip flop U15 pin 5 (sheet 2) and is clocked through to the 'Q' output (pin 1) on receipt of a positive clock pulse from the strobe line. The address coincidence (add-co) pulse will remain active until it is reset by the reset line.

The read/write line from the shift register U4 pin 5 is inverted by U8 and fed to the 'D' input of the 'D' type flip flop U15 pin 9. The strobe line will clock system R/W through to the 'Q' output pin 13. This will be high for a system write (i.e. update an output) with a high on pin 12 for a system read (i.e. reading inputs).

2.2 Ram Update

The circuitry associated with updating the ram is shown on sheets 1 and 2.

The address coincidence and the system read signal are 'AND'ed together to give a module read signal (sheet 2, U2 pin 3, TP35). This signal clocks the monostable U20 producing a positive inhibit pulse of 60 micro-seconds on U14 pin 10. The inhibit pulse is fed back and 'AND'ed with system write by U2 which causes U13 (a line selector) via inverter U21C to select the update address. This channel address is fed to the three RAMs U10 to U12. When writing to an analogue output the Main Controller gives an extra strobe pulse which produces a negative output 'write' pulse. This 'write' pulse clocks the 12 bits of data from U5 and U6 into the three RAMs U10 - U12.

The time between analogue output updates depends on the system configuration. Normally analogue outputs are updated within about 340 m.secs. refer to the FICS-11 Programmer´s Manual for more details about timing.

2.3 Output isolation

2.3.1 Digital drive signals

Isolation of the 12 bit drive signals for the D-A converter U31 is achieved with quad opto-isolators U24 to U26 shown on sheet 3.

Isolation for the multiplex and multiplex inhibit signals is achieved with U27. The rise time of the inhibit signal is ensured to be faster than the multiplex signals by driving pin 8 of U27 hard from two inverters of U23. In addition capacitors C25 and C26 further sharpen the inhibit rise time. The level shifter U32 driving the multiplexers U33 and U34 is used toachieve adequate rise and fall times for the multiplex and inhibit signals from U27 without high current drain from the isolated supply.

The address coincidence signal is isolated by the single optisolator U28.

2.3.2 Isolated supplies for output stages

U29 is an isolating short circuit proof DC-DC converter providing regulated +15V and -15V voltages for the D-A converter U31, its associated buffer amplifiers and multiplexers, the address/voltage monitor and the output stages.

C30 to C36 and L1 to L3 provide low and high frequency filtering of switching spikes within U29 and of common mode interference impressed upon the external connections. U30 is a series regulator providing +5V to supply U31, U32 and the opto-isolator transistors.

2.4 Output Refresh

The circuitry associated with output refresh is shown on sheets 2 and 3.

The outputs are continually being refreshed in order to keep the sample and hold capacitors C56, C60, C64, C68, C72, C76, C80 and C84 at their correct voltages. The rate of refresh is determined by the refresh clock shown on sheet 2 and is formed by U2-B, C24 and R9. This 3 kHZ signal is fed to the monostable U20-B which produces a series of 60 micro-second pulses. These pulses clock the binary counter U22-B whose output gives the refresh address. This address is used to select the current channel data from the RAMs U10-U12 via U13 (on sheet 1).

The -10 volt reference shown on sheet 3 is formed by D5, U35-B and its associated components and is fed to the D to A U31-B pin 17. U31 is a multiplying D to A consisting of 12 CMOS switches and a R-2R ladder and is used in conjunction with U36 to produce a 0..10 Volt output (with LK8 fitted) or a 0..5V output (with LK7 fitted).

2.5 Voltage outputs

The circuitry associated with theses outputs is shown on sheet 3.

Channels 5 to 8 are permanently configured as voltage outputs whilst channels 1 to 4 can be either current or voltage. Channels 5 to 8 are identical and only channel 5 needs to be described.

The buffered D to A output at U36 pin 6 (either 0..5V or 0..10V) is sent to the output multiplexer U34 pin 3 which will update the appropriate channel capacitor. The multiplexer is inhibited during address changes to allow for the settling of the D to A. U42 buffers the incoming voltage on capacitor C72. The output from U42 is fed to output drive transistor Q10.D25 to D28 prevent outputs from U42 to U45 from going too negative.

2.6 Current outputs

The ciruitry associated with the current outputs is shown on sheet 3.

A maximum of four current outputs (channels 1 to 4) can be accomodated. If channels 1 to 4 are not configured as current outputs then they are configured exactly as the voltage outputs for channels 5 to 8.

All current channels are identical and therefore only channel 1 needs to be described.

The input voltage to U38 pin 3 is derived from a potential divider driven from the voltage signal for the voltage outputs (either 0..5V or 0..10V). The output from the potential divider is buffered by U37 which supplies the current signal multiplexer U33. For 4-20mA output ranges the +0,4V offset required at U37 output is generated by R141. R141 and R142 are current and voltage range dependent, see configuration table.

The buffer amplifier U38 and the output drive transistor Q6 operate in the same way as the voltage drive circuit except that the precisely controlled voltage at Q6 emitter is 2V. R68 is shorted with LK C1C and R68, being a precision 100 ohm resistor, causes the collector current output to be 20mA for full output.

2.7 Digital Inputs

All the digital inputs and are shown on sheet 4.

All channels are identical and only channel 1 needs to be described.

The input consists of a rectification diode D29 and a constant current source consisting of Q14, R108, R109, D30 and D31.which supply the opto-isolator U46. The output of U46 is then smoothed by R110, C86 and R111 and is read by the shift register U19-B shown on sheet 2. Normally the P/S line on U19 pin 9 is high, keeping the shift register in the parallel mode. When the main controller requests a read, the shift register is put into the shift mode and the bus transmitter U18-C is enabled by 'input read' from U21-E pin 8 going high. The main controller clocks the data out of U19 and into the D-type flip-flop U17-B via LK1. This flip-flop introduces a one clock delay required by the main controller. The data is then sent down the DECA bus via the transmitter U18. The transmitter is then disabled by a high on the reset line.

Normally links 1 and 4 are fitted and link 2 and 3 omitted.

2.8 Address/Isolated voltage supply monitor

The address coincidence pulses and all voltage rails are monitored so that in the event of a failure the outputs are switched off.

The circuitry comprises Q1 to Q5, RL1 and associated components.

The address coincidence signal to U28 pin 2 is normally kept high by the monstable U16-C via an inverter in U23-B providing the period of the address coincidence pulses is less than 50m.sec. The output of U28 at pin 4 holds the voltage at the junction of R49/R50 high enough to ensure that under normal conditions Q2 is fully switched on.

If one or both of the +15V or -15V supplies fail the current through the chain R53, D8, Q2, D9, D10, and Q3 base will fall to a very low value causing Q2 to switch off.

Q2 switching off causes RL1 to switch off and break the +15Vsupply to the output stages.

If U30 fails the +5V will be too high or to low. If the +5V is too high Q1 will switch on thus switching Q2 off. If the +5V is too low the voltage at U28 pin 4 will be too low and Q2 will switch off.

Because U29 is short circuit proof a short circuit on the output side of RL1 contacts would cause RL1 to switch off and on rapidly. This would cause contact wear and confusing fluttering of the address LED D14 on the front facia unless a slower switching rate could be arranged.

C47 ensures, for all possible short circuit conditions, that sufficient base drive is available for Q4 to quench C49 immediately after a short circuit occurs on the output side of the relay contacts. Q5 switches on again after a short delay when the voltage across C49 reaches about4V.

The "trip and try again" action due to short circuits are identified by the front LED switching at about 200 m.sec. on and 400 m.sec. off.

Note:

Voltage outputs are current limited in their output stages by the resistors fitted in each collector of the output drive transistors. A voltage output short circuit to the return common negative rail will not cause the monitor to drop out.

A power-on reset is provided by R57,R58 and C48 which will disable the multiplex driver until the voltage across C48 has risen sufficiently to enable U32. D11 enables quick discharging of C48 during power-down.

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1 General Description

The Quad Input Isolator module has provision for amplifying up to four isolated low level inputs. The inputs are isolated from system potentials and from one another. Each output is connected to one input of an Analogue Acquisiton module. The channels are hardware configured to give a zero to ten volt output signal for a full scale change of input. Thermocouple cold junction compensation is achieved in the connector block on each input.

Input sensor linearisation takes place in the Analogue Acquisition module, not in the Quad Input Isolator module.

2 Description of circuit elements

Refer to circuit diagram A150055 and PCB assembly AH150055.

Note that in this description integrated circuits have been identified with the prefix "U--", as standard practice, although the prefixes in the circuit diagram here are "IC--". The circuit diagram will be changed to "U--" at the next issue.

2.1 Isolated power supplies for the four isolated input channels

The 24 volt supply for the isolated supplies comes from the system power supply via the edge connector and is regulated by T5 to give a 7.6 volt supply rail to U5, U6 and U7. U5 and associated components form an oscillator of frequency 1.6 kHZ aproximately with a mark/space ratio of about 1 to 20. The output of U5 is inverted by U7 which feeds U6 where the frequency is halved. The 800 Hz signal is gated with the original signal by U7 whose ouputs drive FETs 1 and 2. The FETs are switched on in anti-phase to each other with a dead band period controlled by U5 where neither FET1 or FET2 are on. The two FETs drive the primary of transformer TX1. R60 and C35 damp the voltage overshoot when both FET's are off.

The secondary of the transformer supplies the four identical isolated power supplies. Each channel consists of an isolated secondary supply from the transformer which is rectifies by D1 to D4 to produce unregulated +20 volts. The +10 volt rail is regulated with respect to the 0 volt rail by U1. This is achieved by dividing down the voltage by R6, R7, R8 and P1 and comparing it with a high stability zener diode Z1. The 0 volt rail is regulated with respect to the - 5 volt and +10 volt rails. This is achieved by dividing by three the diffence between the +10 and the - 5 volt rail and comparing the result with the 0 volt rail.

Adjustment of the supply rails is achieved by P1. This adjusts the +10 volt rail which in turn alters the 0 volt rail. The +15 volt rail is unregulated.

2.2 Arrangement of input compnents

2.2.1 Thermocouple input

The following components are form the input circuitry

R12, R14, R15, R16, R7, R19, R22, R23, R24, R25, R26,, R27, R28, R29, R30, R33, R61, R62, R63, R64, R65.

P4, P5, C6, C7, C8, C9, C10.

Some of these components might be links or might-not be required, depending on the type of thermocouple and the range.
The thermocouple is connected across terminals 1 and 2 (pin 1 being negative). Cold junction compensation is provided by a hybrid circuit inside the connector block. The hybrid uses terminals 3 and 4 as a suppoly and injects current into pin 1. This current varies with temperature. As the temperature in the block changes it produces an offset voltage change across R65/R15. This change in voltage cancels the change in emf due to the thermocouple compensation lead/copper junction at the screw terminals.

The compensated thermocouple input is filtered by R23, C9, R24 and C10 and fed to the non-inverting input of the op-amp U2.

Thermocouple break protection is provided by R61 - R64. R61, R62 and R63 are fitted for upscale protection and R62, R63 and R64 are fitted for downscale protection

2.2.2 4 wire R/T input

The following components form the input circuitry

R14, R16, R17, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R33, R61, R63

P3, P4, C7, C8, C9, C10

Some of the components might be links or might not be required, depending on the range.

Terminals 2 and 4 sense the voltage across the resistance sensor and terminals 3 and 1 provide the measuring current. The current is set up by R14, R16 and R17 and P3 balances this current down to the negative rail. The negative end of the sense voltage is connected to ground while the positive is connected via R19 to the filter circuit of R23, C9, R24, C10. The nominal voltage produced by The R/T sensor is offset by R30, R29, R26 while P4 provides the zero adjustment. The gain of the amplifier is governed by R27, R33, R26, R29 and P5. P5 provides a small gain adjustment.

An upscale break protection based on sensing an open circuit of the R/T bulb current is provided by R61, R62 (two diodes) and R63.

Note: comprehensive break protection of all possible combinations of breaks is not provided.

2.2.3 3-Wire input

The arrangement of the input components on the board is the same as that for the 4-wire arrangement. Externally however terminals 1 and 2 must be connected together to provide the current supply positive for the R/T.

2.2.4 Millivot input

The following components form the input circuitry

R14, R15, R16, R17, R18, R19, R22, R23, R24, R25, R26, R27, R28, R29, R30, R33, R61, R62, R63, R64

P4, C6, C7, C8, C9, C10

Some of these components might be links or might not be required, depending on the range.

The linear input is connected across terminals 1 and 2 (pin 1 being the negative). The input voltage is fed to filter network R23, C9, R24, C10 which is then amplified by U2. The gain of U2 is determined by R27, R33, R25, R26, R29 and R5. The gain is adjusted by P5. An offset voltage introduced by R15 and R16 is taken out by R30, R29 and R25, R26 and P5. The zero is adjusted by P4.

Upscale or downscale protection for mV inputs is formed by R61 to R64 as for the thermocouple inputs.

2.2.5 Volt input

The arrangement of the components on the board for high level volt inputs is the same as the arrangement for mV inputs except that the ratio R18 to R19 is selected to potentially divide down the high level voltage to a suitable low level mV.

Input break profection is not provided for voltage inputs as the potential divider prevents this.

2.2.6 Milliamp input

The arrangement for a milliamp input is the same as that for a voltage input except that R18 is fitted to transpose the mA source into a mV signal.

Input break detection is not provided for mA inputs.as R18 prevents this.

2.3 Input amplifier

U1 and associated components form an amplifier which amplifies the input low level mV signal to approximately 0...10V output at the junction of R40/R42. No offset adjustment is necessary with the LH0044 part-used for U1 as this is a high precision, high again, or low offset voltage, low drift, low input current and low offset current device.

The low level input is applied to the non-inverting input pin 3 through a double stage filter R23/C9 and R24 C10 which reduce series mode ripple or noise on the input signal. The gain of the input amplifier is determined by feedback through R27 and R33 which is potentially divided down by R25, R26, R29 and P5. Gain adjustment is made with P5 and zero adjustment with P4 through R28-1 and R28-2.

The input signal can be positively offset with R14 and R16 and negatively offset with R30-1 and R30-2.

R31, R32 and C11 as well as R38, R35 and C15 are fitted to improve immunity to inteference.

C13 is fitted to reduce the noise badwidth and C12 is fitted to improve the power supply rejection ratio. R14 is not fitted but is provisoned for should devices other than the LH0044 be fitted, see circuit diagram or parts list.

To improve drift performance the amplifier is.thermally shielded with copper tracking around U1 as shown in the shaded area on the circuit diagram.

2.4 Buffer isolator

The output from U2 is fed to the non-inverting input of U3. TX2 and C24 form a resonant circuit whose oscillations are maintained by the feed back path of C23 to the base of T2.

The amplitude of the oscillations is governed by the voltage on the collector of T2 and the current in the base of T2. The amplitude of the oscillations is monitored by a secong winding on transformer TX2 (pins 6 and 5), the voltage of which is rectified by T3. The output of T3 is smoothed by C25 and used as the negative feedback for U3.

Stability of the oscillations around TX2 is achieved by T2 going into saturation which then limits the amplitude of the oscillations. C19 and C20 provide ac stability of the overall feedback loop.

2.5 The Output stage

A third winding on TX2 (pins 4 and 3) provides an isolated output voltage. This winding and the loading on it are identical to the feedback winding 5 to 6 and its loading. Hence the amplitude of the output voltage is identical to that of the feedback voltage to U3 which in turn is equal to that of the output of U2. The voltage is rectified and smoothed by T4 and C26. U4 buffers this voltage and the output is limited by Z3. The common line voltage floats from the analogue ground rail with D5 and D6 acting as clamps.

2.6 Input amplifier resistor calculations

Gain Calculations.

Let RA = 1 / (1/R26 + 1/R29 + 1/R30)

Ignore R28 and P4 as far as gain calculations are concerned

Let RB = R27 + R33 + R40

Min Gain (R27 joined to R26).

Let RC = RA x (P5 + P25) / (RA + P5 + R25)

V TP 18 = Vout x RC / (RC + RB)

Min Gain = Vout/Vin = RC (1 + RB/RC)

RB = RC x (min gain - 1)

Max Gain (R27 joined to R25)

RD = ((RA + P5) x R25) / (RA + P5 + R25)

V TP 16 = Vout x RD / (RD + RB)

V TP 18 = Vout x RD x RA / ((RD + RB) x (P5 + RA))

Gain = (RD + RB) x (P5 + RA) / (RD x RA)

Gain Ratio

Providing RB/RC is much greater than 1 (10 or more) and RB/RD is much greater than one:

Gain Max / Gain Min = 1 + (P5/R25) which is independent of RA.

Offset Calculations

Ignore R27 and R33 (given that Vout is zero at min scale).

Min offset at TP18 = Vsupply x RC / (R30 + RC)

Max offset at TP18 = min offset (1 + R30/R28)

Typical Values

RA = 100R
P5 = 100R
R25= 1 K

Gain

With the above values RC = 91.67R

Min Gain = Vout / Vin = (1 + RB / 91.67).

RB = 91.67 (min gain -1)

Where RB is in ohms.

With the above values RD = 166.7R

Max Gain = Vout / Vin = 1 + (200 x RB / 16670).

With the above values the potentiometer adjustment will be +/- 5%

Offset

Min Offset = V suply x 91.667 / (R30 + 91.667)

R30 = (916.x 67 / Min Offset) - 91.667

Max offset = min offset (1 + R30/R28)

R28 = R30 x Voff(min)/(Voff(max) - Voff(min))

where R28 and R30 are in ohms and all voltages are in volts.