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1 General description

The 6809 microprocessor in the Main Controller controls four ports for:

Communication to the Operator Panel via the panel bus ("S" bus).

Communication to the Analogue Acquisition module via the Analogue Acquisition bus ("M " bus) on the rear flatband cable.

Communication to other modules via the system DECA bus ("L" Bus) on the rear flatband cable

Communication to external supervisory computers, either an isolated RS232 link or an isolated RS422 link.

In addition the Main Controller has 8 isolated open-collector digital outputs for driving external devices.

Memory is divides into 3 areas: firmware, userware and system memory. The firmware comprises the permanent FICS-11 program in EPROM. Userware may be stored permanently in EPROM or alterable in RAM. System memory is always in RAM.

A battery backs up RAM memory when the mains supply to the FICS-11 is switched off. Circuitry to detect a 5V supply failure, an, impending power-down, a battery voltage failure and failure of basic software procedures is implemented to ensure system integrity.

2 Description of circuit elements

Refer to ciruit diagramm AI 150052 and PCB Assembly AH 150052.

2.1 Memory organisation

The total addressable memory space of 64 Kilobytes (KB) is divided up as shown in the memory map in Fig. 1.

System RAM occupies the space from 0000 to 3FFF. Two 8kb RAM devices (U6 and U5) are always fitted.

Userware can occupy up to 24KB of space starting at 4000 and ending at 9FFF. U4 will always be fitted whereas U3 (and U2) are required only when the Userware does not fit into one (or two) 8K devices. Link 1 must be fitted for EPROM based userware whilst Link 2 must be fitted for RAM based userware.

The firmware occupies the high end of memory from A020 to FFFF. The small area from A000 to A01F is reserved for enabling input/output communication parts U14, U15 and U16. The small area from FFFO to FFFF is used for the interrupt vectors in the microprocessor U20.

All memory parts except for the firmaware are 8KB devices.

The firmware resides in one part only, either a device of 16KB or 32KB size, and either type can be fitted without the need for harware link changes. To date the firmware is less than 16KB in size and a device of 16KB is normally used. Future revisions to the firmware could mean that the firmaware exceeds 16KB and will therefore fit only in a 32KByte device. It can be seen from the memory map, however, that firmware may not exceed 24KB in size where the bottom 8KB of a 32KB part will never be addressed.

Note:
PCB tracking has been provided to allow userware to be plugged into a socked PL1 on the front of the Main Controller. The mechanics, however, has not yet been implemented.

2.2 Address decoding

Because only 8KB memory devices are used, (except for firmware), address decoding for enabling the memory devices is simple. U7 decodes the top address lines A15 to A13 which together with the VMA (Valid Memory Address) from U20 via U10 and/or U13 cause one of U1 to U6 memory parts to be enabled by a pull-down chip enable signal on pin 20 from the respective output at U7.

U1 is inhibited in the small range from A000 to A01F which is used for the communications and versatile interface adaptor parts U14, U15, U16 and U17. The address decoding to achieve this is accomplished by U9-B, U11-B, U11-C, U22-C, U12-B, U13-B and U12-C. Adresses between A000 and A01F will cause the outputs of U12 pin 4 to be high, thus inhibiting the output of U1 in this range. Due to the action of the signal from U13 pin 11 U9 will be enabled whilst U1 is inhibited. One of the communications devices U14, U15 or U16 will be enabled in the range A000/1, A002/3, A004/5 according to the state of the address lines A1 to A4 on the inputs of U9 pins 1 to 4.

The address range A006/7 is used to enable the transparent latch U8 to toggle its Q8 output on and off with the D7 data bit on U8-B pin 18 during communications transactions. Q8 is drives Q1 and D1 to indicate communications activity on the front panel and to enable Tx of the RS-422.

U17 is enabled when pin 23 is low and pin 24 is high, i.e. between A010 and A01F within the reserved address range for the Input/Output.

2.3 The microprocessor

The address lines A0 to A15 are buffered by the tranceivers U18-B and U19-B. These are permanently enabled and are arranged to have a fixed direction flow from port B to port A. to achive a timing accuracy of better than 1 second per day over the whole working temperature range the 8Mhz crystal XL1 is a selected device which is further trimmed on test by C15b.

The data port D0 to D7 is buffered by the tranceiver U21-B, the direction of data through U21-C being determined by the R/W signal from the microprocessor.

The microprocessor inputs MRDY, BREQ and HALT which are not required for FICS-11 are permanently inactivated by pull up resistors R13 and R15.

The E clock is buffered by U10-C and a buffered VMA (Valid Memory Address) signal is dervied by ANDing the E and the Q clocks.

The RST (Reset) signal to U20-B pin 37 is derived from the monitoring circuitry to be described later. A low input lasting longer than one bus cycle will reset the processor.

There are three levels of interrupts used in the FICS-11 main controller module. The highest priority interrupt is the Non-Maskable Interrupt (NMI) at U20 pin 2. The next level is the Fast Interrupt Request (FIRQ) at U20 pin 4 followed by the Interrupt Request (IRQ) at U20 pin 3.

The NMI is attached to a harware timer in U17 which has a period of 20ms. The 20ms interrupt provides the time reference of the Main Controller. The NMI simply responds to the interrupt, updates a counter (used for the updating of time variables) and schedules an IRQ to occur.

FIRQ is used solely by the communication drivers U14-B, U15-B and U16-B. This enables all the data transfers to and from the three ACIAs to occur under interrupt control. The ACIAs handle serial communication between the Main Controller and the Operator Panel, The Analogue Acquisition module(s) and an external computer. The data from a completed Analogue Acquisition card transaction is processed in the foreground under IRQ. Completed messages from either the Operator Panel or the computer are processed in the background (not under interrupt).

There are two souces of IRQ ,one from the NMI routine (timer) and one from the Analgue Acquisition module communications driver running under FIRQ. The timer driven IRQ checks the power fail line and a power down sequence is executed if an impending power down is detected. It then schedules a communications transaction with the first analgue card and does all other input and output.

The two IRQ signals from U17 are ANDed by U10-B before being routed to U20-B pin 3.

2.4 Communications

Communications to an external computer, the Operator Panel, the Analogue Acquisition module(s) and other (dumb) modules take place over the external link, the Operator Panel bus, the Analogue Acquistion bus and the DECA bus respectively as shown in Fig. 2.

The Operator Panel, Analogue Acquisition and external supervisory equipment communication is achieved through the Asynchronous Communications Interface Adapters (ACIAs) U14, U15 and U16 dedicated to these tasks.

At the FICS-11 data bus interface an ACIA appears as two addressable memory locations. Internally there are four registers, two read only and two write-only registers. The read-only registers are Status and Receive Data; the write only registers are Control and Transmit Data. The serial interface consists of serial input and output lines, with clocks, and three peripheral/modem control lines.

The ACIAs are enabled with signals generated in U9-B. Register pair select within the device is determind by the address line A0. The R/W signal determines which of two internal registers is written to or read from.

The 4.9152 Mhz oscillator comprising XL2, U28-E and -F and associated components is divided down by flipflop U25-b and -C and counter U26-B to provide the clock rate for the ACIAs.

Serial transmit and receive actions take place under the control of the internal status and control register at a speed determind by the clock rate connected to poins 3 and 4.

The clock rate to pins 2 and 3 of the ACIAs is divided down by a factor determind during system power-up by bits set in the control register of the ACIA. In FICS-11 the rate is divided down by 16. This enables incoming asynchronons serial information to be synchronised, read and bus organised for transfer to RAM buffers. Outgoing information is organised for serial transmission after being received from RAM buffers.

The Panel and Analogue Acquisition communications rate is fixed at 9.6Kbaud whilst the external communications baudrate and clock rate depend on the setting of SW2.

Standard RS-422 components U29-B, U30-B, U31-B and -C and U32-B and -C are used to couple the signals between the Panel Analogue Acquisition ACIAs to the back ribbon cable bus between modules. The external communications signals TX3, and RTS from U16-B pins 6 and 5 respectively are coupled to the non isolated side of the opto-isolators by U28-C and -D and pull up resistors R85 and R84. Received signals RX3 and CTS are passed straight to U16-B from the receive opto-isolators and pull up resistors R86 and R83.

U17-B , which is enabled between A010 and A01F, controls the DECA bus transactions. RS0 to RS3, (pins 38 to 35) determine which internal register is addressed. The ø2 clock input to pin 25 is dervied from the microprocessor E signal and controls the rate at which transactions on the black ribbon cable take place. The 2Mhz rate of the E (and ø2) signals provide the timing for the DECA bus transactions to take place at 500Khz clock rates. The DECA bus clock and data signals are transmited via RS-422, parts U31 -B and -C and U32-B and -C whilst the reset and strobe signals are sent with TTL part U22-E and -D. The timings for the DECA bus reset, clock, data strobe and R/W signals are shown in Fig. 3. with further examples recorded from actual transactions shown in Figs. 4 to 10.

Note: the DECA bus transactions take place for a relatively short time every 20 m.sec.as indicated in Fig, 4. Not all transactions take place every 20 m.sec. Some modules are updated over many 20 m.sec.cycle periods depending on system complexity. However, all digital inputs are acquired every 20 m.sec. For more information about the software organisation of DECA bus tranactions refer to the FICS-11 Programmer's Manual in the section dealing with timing details.

Q2, R18, R19 and tracking to the back ribbon cable wire 10 has been made to provision for possible address acknowledgement from other modules. This has, however, not yet been implemented.

2.5 Versatile Input/Output Interface Adaptor (VIA)

The VIA U17-B controls the following functions:

the communication transactions on the serial DECA bus to the Analgue Output,Solenoid Driver and Relay Output modules.

the digital outputs within the Main Controller module.

the monitoring of basic functions within the Main Controller. In the event of a failure either watchdog and/or system alarms will occur.

the generation of interrupt NMI which provides the time base reference.

the reading of system address switches for the external communications link.

2.5.1 DECA bus transactions

These have already been described above in the section describing communications.

2.5.2 On-board Digital outputs

Data for the digital outputs is transmitted by the DECA bus and clocked into the input register of U35-B via the two 4-stage shift registers U34-B and -C The input register of U35-B is strobed to the output by the strobe signal U33-B pin 13. The outputs of U35-B are buffer inverted by U36-B, the outputs of which drive the opto-isolators U46, U47. RP3 and RP4 are fitted to prevent the small leakage currents of U36 outputs in their off state from passing through the LEDs of the opto-isolators.

2.5.3 Monitor inputs/outputs

The internal battery status signal applied to U17-B pin 14 is generated after U17-B sends an output signal BAT TEST from pin 13 to the battery monitoring circuit. The monitoring circuit will be described later. The internal battery status is normally high but will be low if the battery voltage is too low. A low battery voltage will cause a system alarm. Provision has been made to test a battery fitted on an external PCB plugged into PL1. However the mechanics has not yet been implemented and so the external battery status signal to U17-B pin 15 has been pulled high so that this input does not unecessarily cause a system alarm.

The Power Fail signal from the Power Supply Unit is fully described in the technical description of the Power Supply Unit. The Power Fail signal will go low within 13msec of switch-off of the mains supply. The 5V supply will remain stable for at least a further 40 msec. After receipt of a Power Fail signal going low U17-B will cause an IRQ to the microprocessor. The microprocessor completes ist shut down routines before the 5V drops out of specification.

If the microprocessor does not successfully complete its background cycle it will not reset one of the timers in U17-B. A time overflow will cause the output of U17-B pin 6 pulse the watchdog line. The watchdog will cause resets to the microprocessor as described later.

2.5.4 Non Maskable Interrupt (NMI) signal

Another timer in U17-B is configured to be free running and will transmit a square wave signal with a period 20msec from pin 17 to the NMI input of the microprocessor to provide the time base reference for the whole system.

2.5.5 System address

When closed SW1 contacts pull down the inputs to U17-B pins 2,3,4 and 5. The pattern will be recognised at start up by U17-B and transmitted to the microprocessor. All FICS-11 system backplites and later versions of some FICS-10 backplates are fitted with a coding switch. A switch. in a backplate operates in parallel with a switch SW1 on the PCB.

Note:

When a switch contact is closed, either the internal switch SW1 or the external backplate coding switch, the other switch in parallel is ineffective. It is preferable to set system addresses with the external switch in the backplate and to leave SW1 contacts on the board open.
SW1 has been fitted on the PCB in FICS-11 to make it plug-in compatible (harware only) with original FICS-10 Main Controllers where there was no provision (no contacts) for an external system coding switch. SW1 on the board is no longer required for FICS-11 and will probably be removed in the future.

The external backplate switch has more than four positions. Only the four positions connected to U17 pins 2, 3, 4 and 5 are effective, giving a maximum number of system address of 16.
The switch positions are read at system power-up only.

2.6 Monitoring circuitry

2.6.1 5V Supply

U23 is arranged to detect the 5V supply voltage and cause a reset to the microprocessor if the voltage is not grater than 4.75V. Hysteresis of the switch action is approximately 0.08V meaning that the voltage will have to increase to more than 4.8V before a non-reset condition is re-established. U23-B also provides overvoltage resetting. A reset will also occur if the 5V supply exceeds 5.25V to 5.5V. Hysteresis for over-voltage is also approx 0,08V. Normally the output at U23-B pins 1 and 7 will be high causing Q3 collector to be low. If the 5V is out of tolerance U23 pins 1 and 7 will go low and Q3 collector will go high resetting U24 and switching Q4 on.

Without the pulsed input through D7, Q9 and Q10 form a threshhold switching circuit with hysteresis. Q10 will switch off when the input to R48 is less than about 2.8V and will switch on when the input exceeds about 3.3V

Q4 collector falls rapdly when Q3 switches off and causes an immediate reset to the microprocessor through R59. When the 5V is re-established the collector of Q4 rises slowly so that there is about a 0.5sec. delay in removing the microprocessor reset. This delay is to allow the power supplies in the whole system to settle before the microprocessor is released. Q11, R 55 and U27-C form the drive for the RED LED watchdog lamp. The lamp illuminates when a microprocessor reset is applied.

During the time the 5V is out of tolerance Q5 and Q6 are switched off. During this time the battery will supply power to the RAM devices U5-B and U6-B (always) and U2-B, U3-B and U4-B (if configured as RAM) via LK6 and D2.

To protect the battery LK7 is fitted instead of LK6 until the system is to be commissioned. On commissioning LK7 replaces LK6 so that the battery provides back up for RAM devices.

Q8 (and therefore Q7) are normally switched off. Every few minutes a BAT TEST signal from U17-B will switch Q8 on. Providing the battery voltage is at least 2.6V Q7 will also switch on causing the INT.BAT.STATUS signal to go low. If the battery voltage drops to somewhere between 3.1V to 2.6V Q7 will not switch on and the INT.BAT.STATUS signal will be high, causing a system alarm. The guaranteed minimum data retention supply voltage for the RAM devices used is as low as 2.0V.

D2 prevents the 5V being applied to the battery when the 5V supply is within nomal tolerance and D3 prevents backwards base/collector discharge current in Q7 when the equipment is switched off.

2.6.2 Watchdog

Providing the microprocessor completes is background cycle successfully pulses will be received at U-28-G pin 13. The pulses are differentiated and passed via D5 to the reset input of U24-B, a binary counter. The clock input to U24-B is derived from U26 pin 1, which outputs a fixed frequency divided down from the communications oscillator. Before the count reaches U24-B pin 14 the watchdog pulses to U24 will reset the count to zero. if the processor fails to complete its background cycle the watchdog pulses will stop and U24 pin 14 will go high after about 1.7s switching Q10 off for about 5 msec. thus causing a reset pulse.to the microprocessor. U24-B will continuosly count round with a period of about 3.4 sec. until it is reset.

2.7 Output power-up delays

2.7.1 Digital output delay

Digital outputs are inhibited after the microprocessor is released by approximately 0.2sec. until filter R57, C33, allows the enable pin of U35-B pin 15 to reach its enable threshold. This is to gave the microprocessor enough time for the digital output registers to be loaded with their correct values.

2.7.2 RS-422 External Communications delay

The transmit channel of the RS-422 external communications link is inhibited for a few milliseconds after the microprocessor is released by filter R58 C34 so that spurious signals are not transmitted.In addition when RS-422 external communication is not required the COMMS DEL signal is be held low by the 0V connected to U27-E pins 12 and 13 by LK16. In this way the Tx output of the RS-422 is permanently held in the tri-state condition and will not contend with other equipment possibly still connected to it.

2.8 Isolated Outputs

2.8.1 RS-232 Communications

U37 provides an isolated short circuit proof +/-12V supply. C57 and C58 provide additional spike quenching and L1, L2, L3 and L4 block common interference. U48 provides the 5V required by U49 and the opto-isolators.

U49 is a triple driver/receiver. The receiver channel inputs Rx and CTS are loaded by R105 and R106 which provide the RS-232 line termination impendance required R103, R104 and D15 to D18 provide input networks to quench spikes.

The Outputs are protected by D19 to D22 in Conjunction with small resistors R107 and R108.

On the opto-isolator side R97 and R98 provide the opto-isolator pull-up loads and R93 to R96, R99 to R102 and C64 to C67 provide further small fittering of input and output signals to further prevent noise from causing false transactions.

2.8.2 RS-422 Communications

U42 provides an isolated short circuit proof 5V supply for U50 configured as a driver and U51 configured as a receiver. L5 and L6 are to block common mode interference.

On the PCB at the terminal block the driver and receiver are termited with RT5 and RT6 respectively as standard. RT1, RT2, RT3 and RT4 are provisioned for termination in special circumstances (see RS-422 standard or communications applications reports).

R111 and R112 provide pull up and pull down of the receive inputs in the event of open inputs. R109, R110, R113, R114 and D23 to D28 provide input and output protection against spikes impressed on the external wires.

R91 and R92 are the pull up loads for the TxEn and Tx signals and RP7, RP8 and C71, C72 and C81 configure U51 and U52 and provide additional small filtering against noise.

Isolation between the RS-422 communications link and the digital outputs can be arranged by not fitting LK22 and LK25.

2.8.3 Digital outputs

The supply necessary for the opto-isolators U46 and U49 and output driver U52 can be provided by the RS-422 5V supply when LK22 and LK25 are fitted. Alternatively when the RS-422 and Digital outputs are required to be isolated from one another the supply can be provided by an external + supply to termina 11 and a -. supply to one of terminals 1 to 10.

Links LK22 to LK27
The output signals transmitted across U46 and U47 switch logic "highs" to their respective output driver. L7 and L8 block common mode interference, RP5 and RP6 provide further blocking in the opto-isolator lines and RP5 and RP6 in conjunction with respective capacitors C73 to C80 provide further small filtering of noise.

D29 and D30 prevent overvoltage spikes from damaging U52 output transistors but do not provide protection against a permanently applied overvoltage.

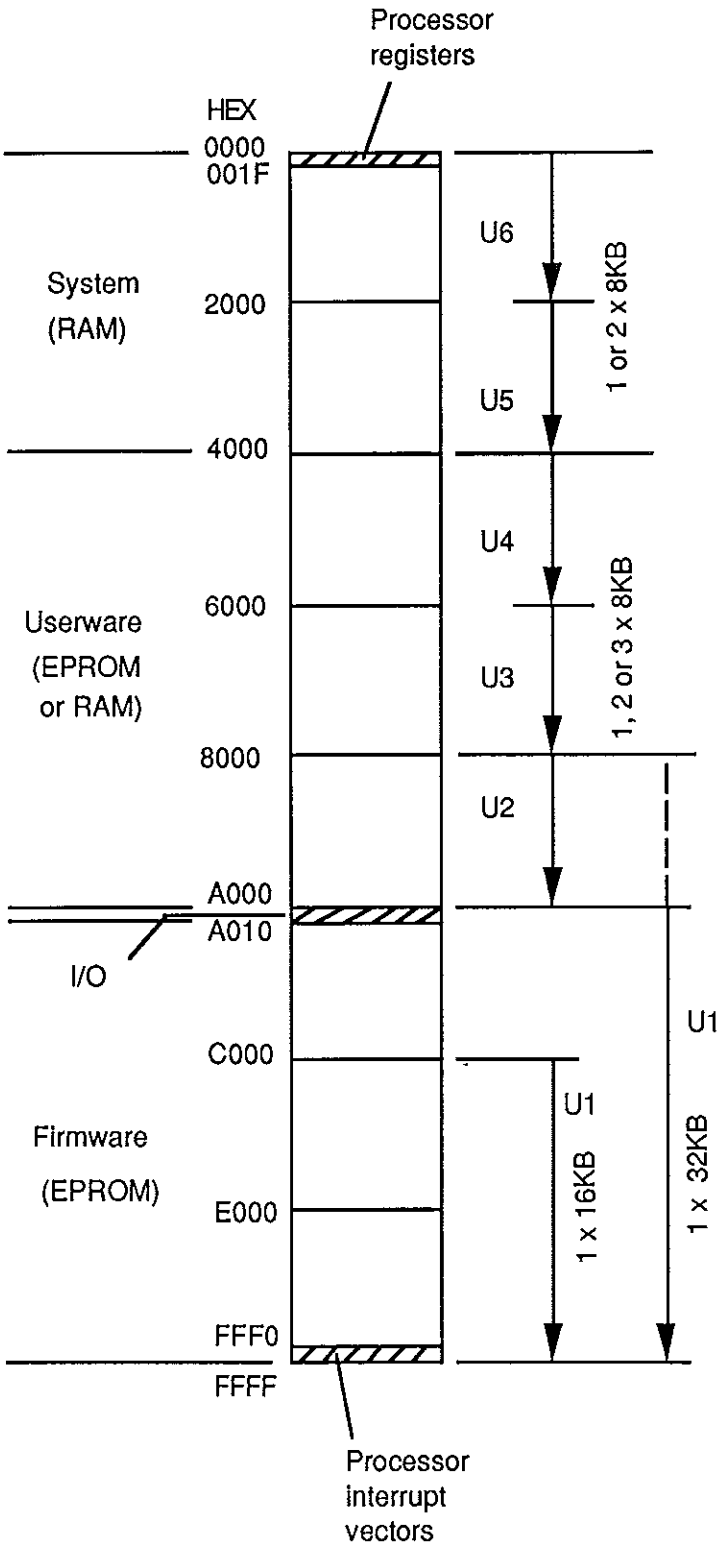

Fig. 1 Main Controller memory map

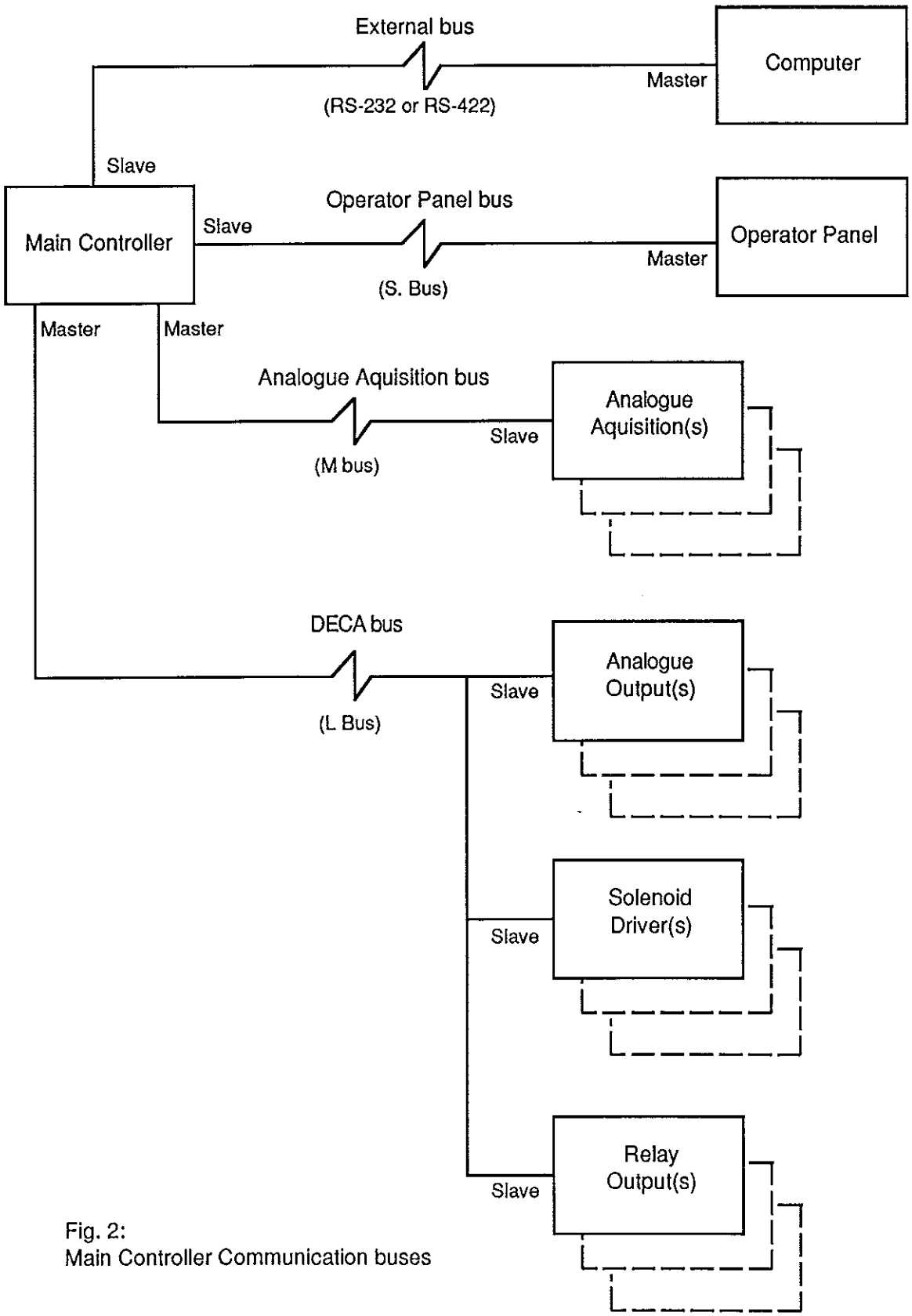

Fig. 2:
Main Controller Communication buses

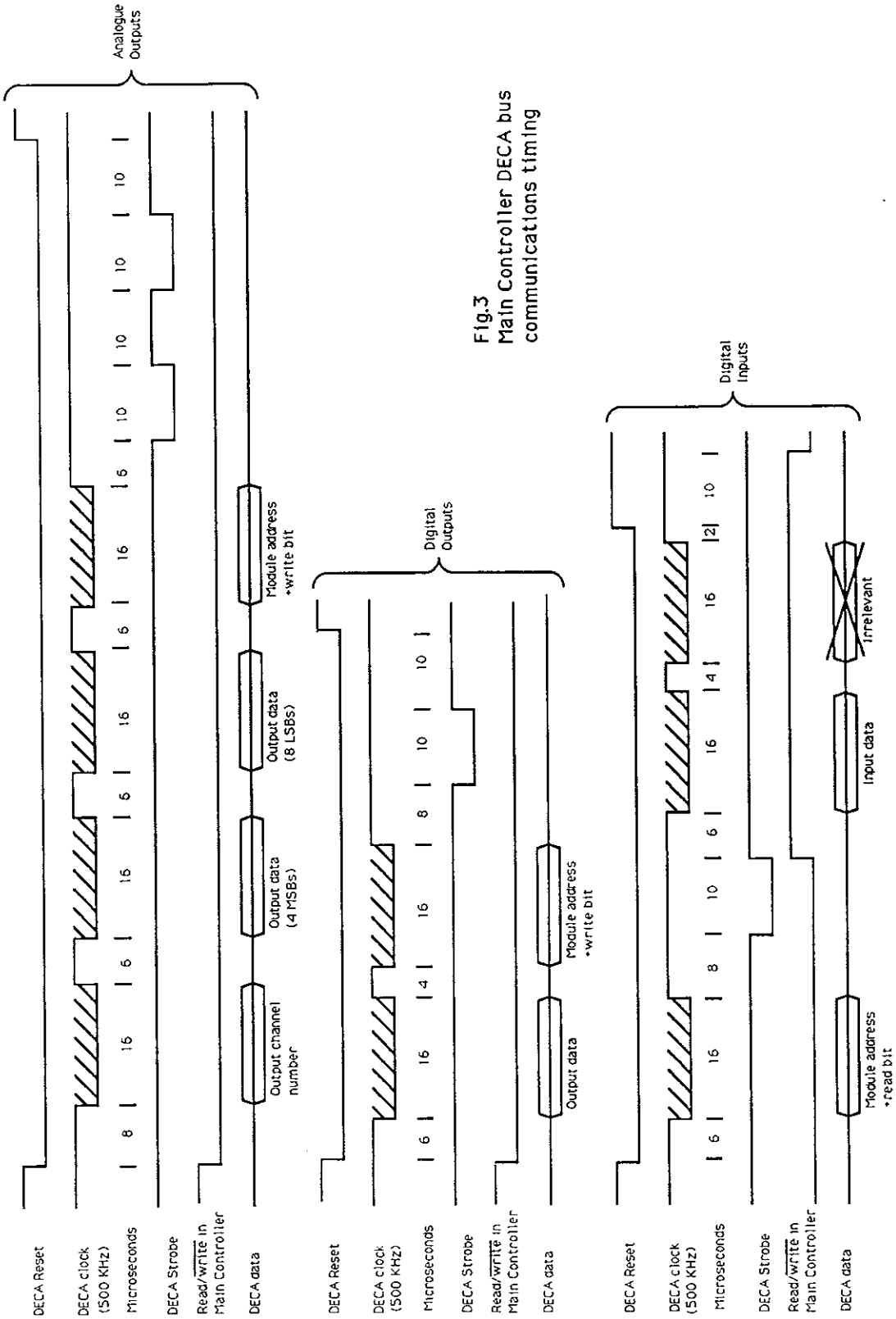

Fig.3
Main Controller DECA bus communications timing

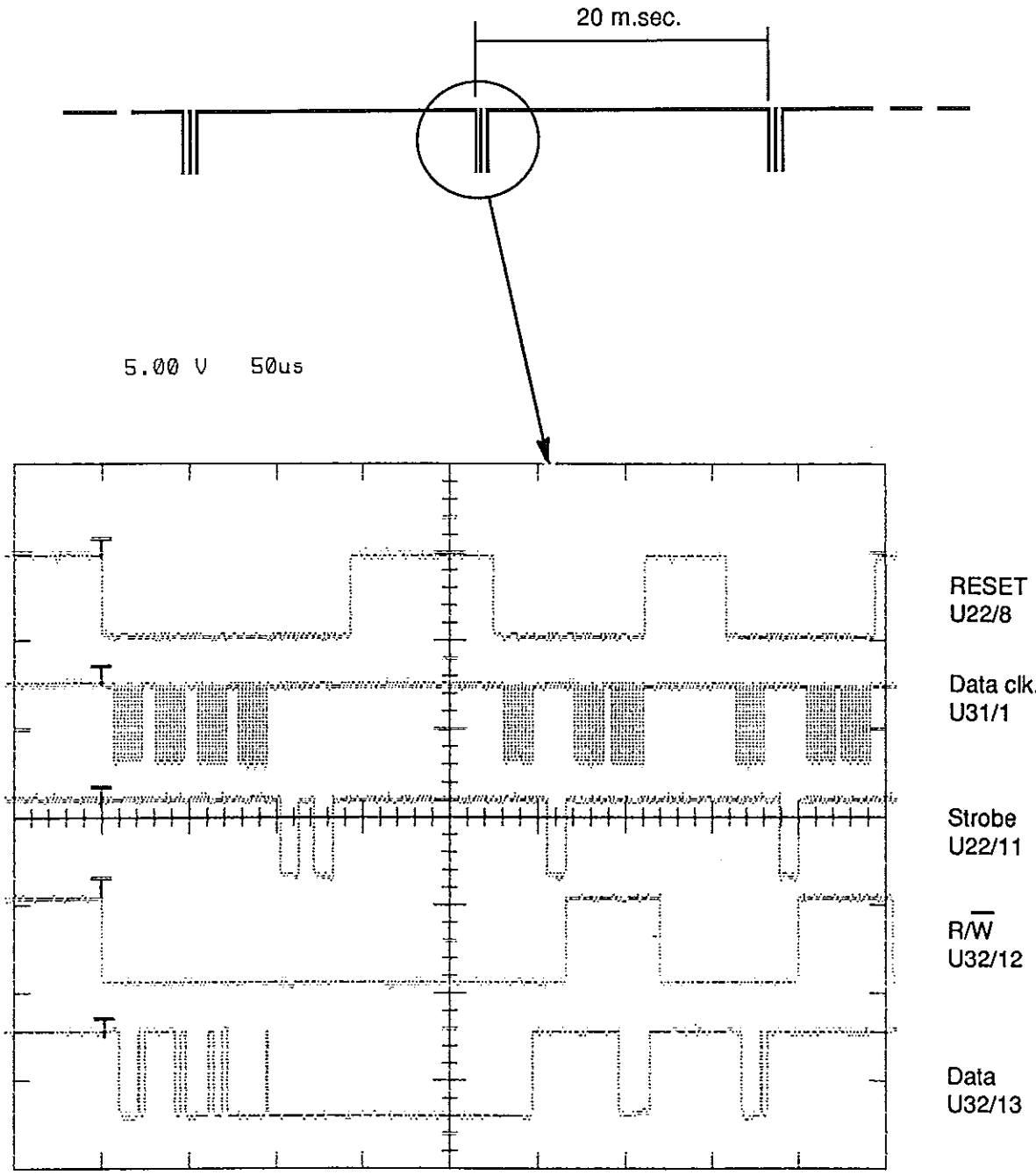

Fig. 4 Analogue Output and Digital Input transactions

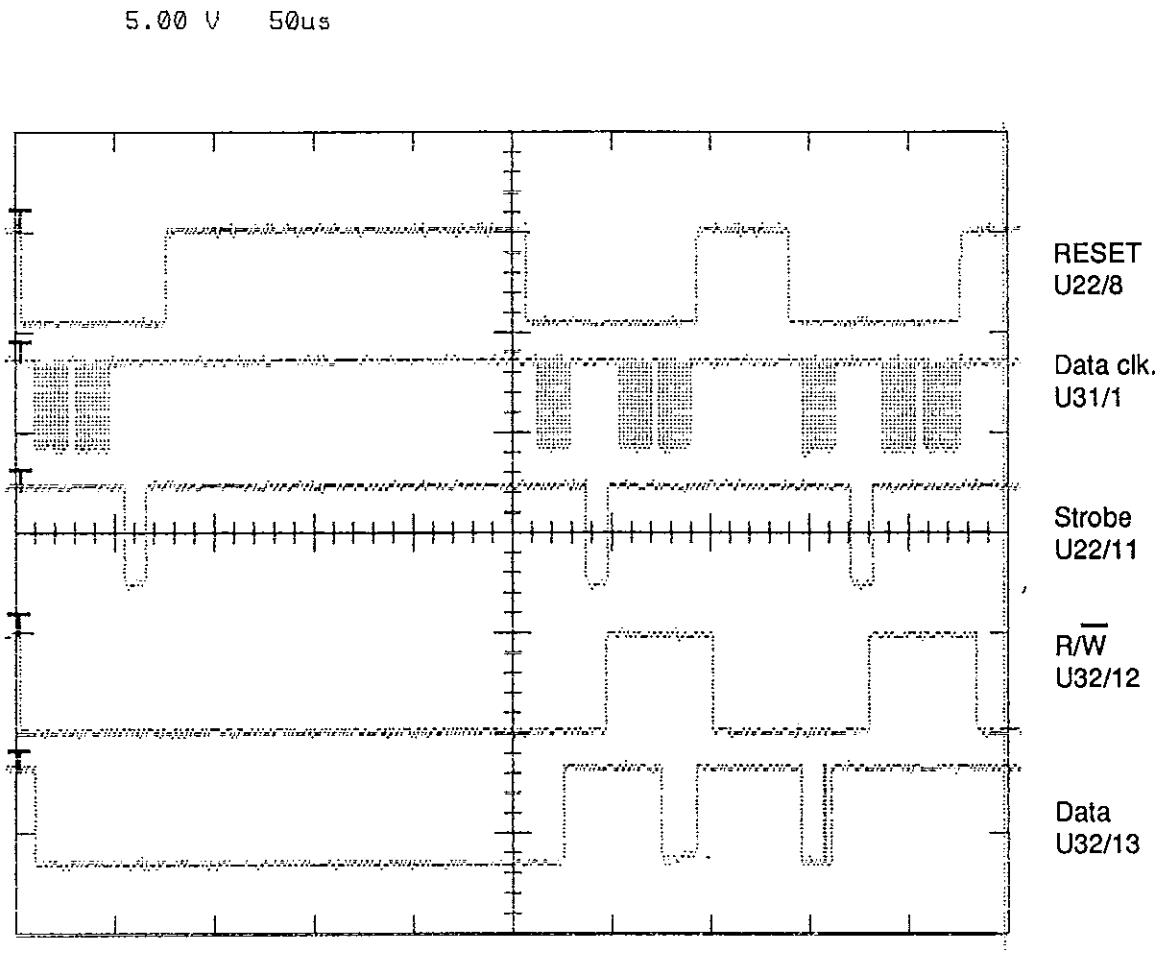

Fig. 5 Digital Output and Digital Input transactions

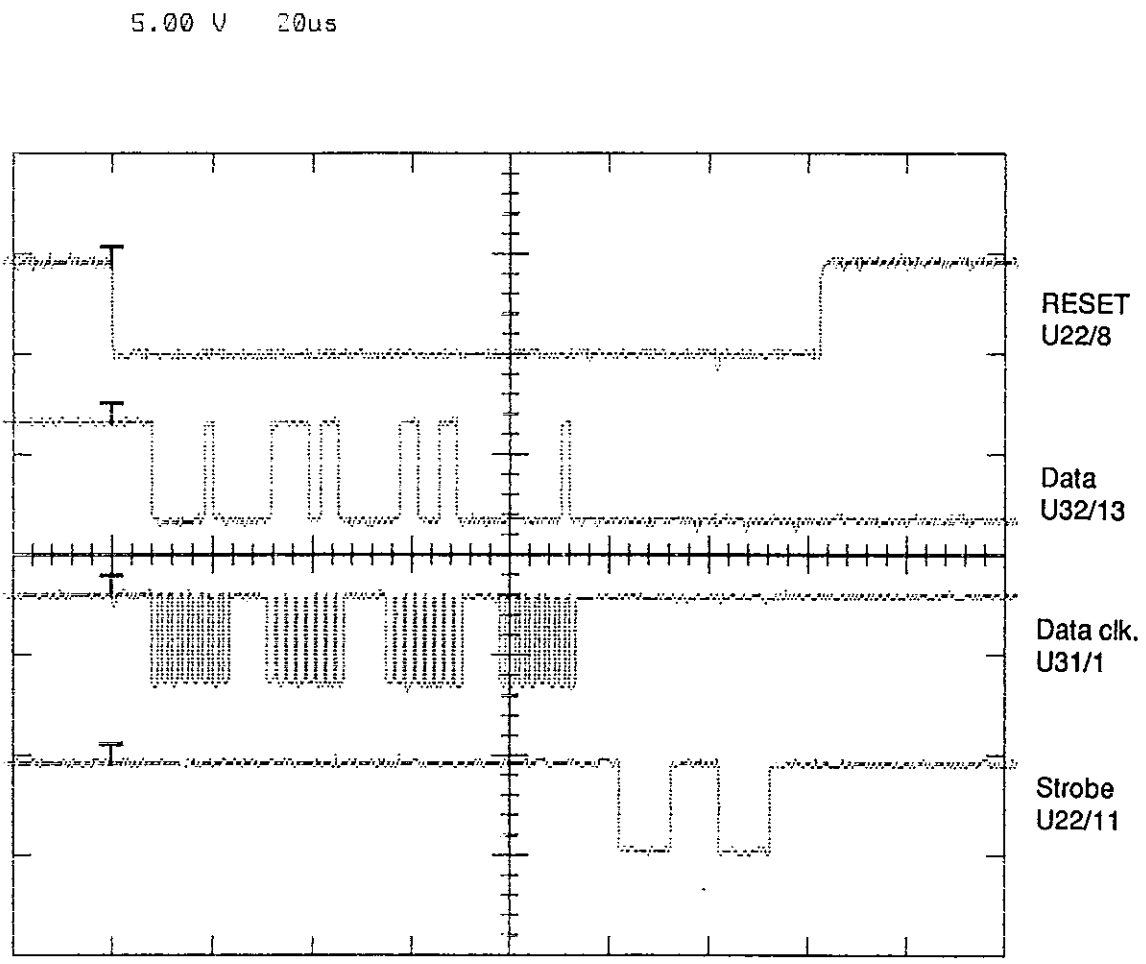

Fig. 6 Analogue Output transaction

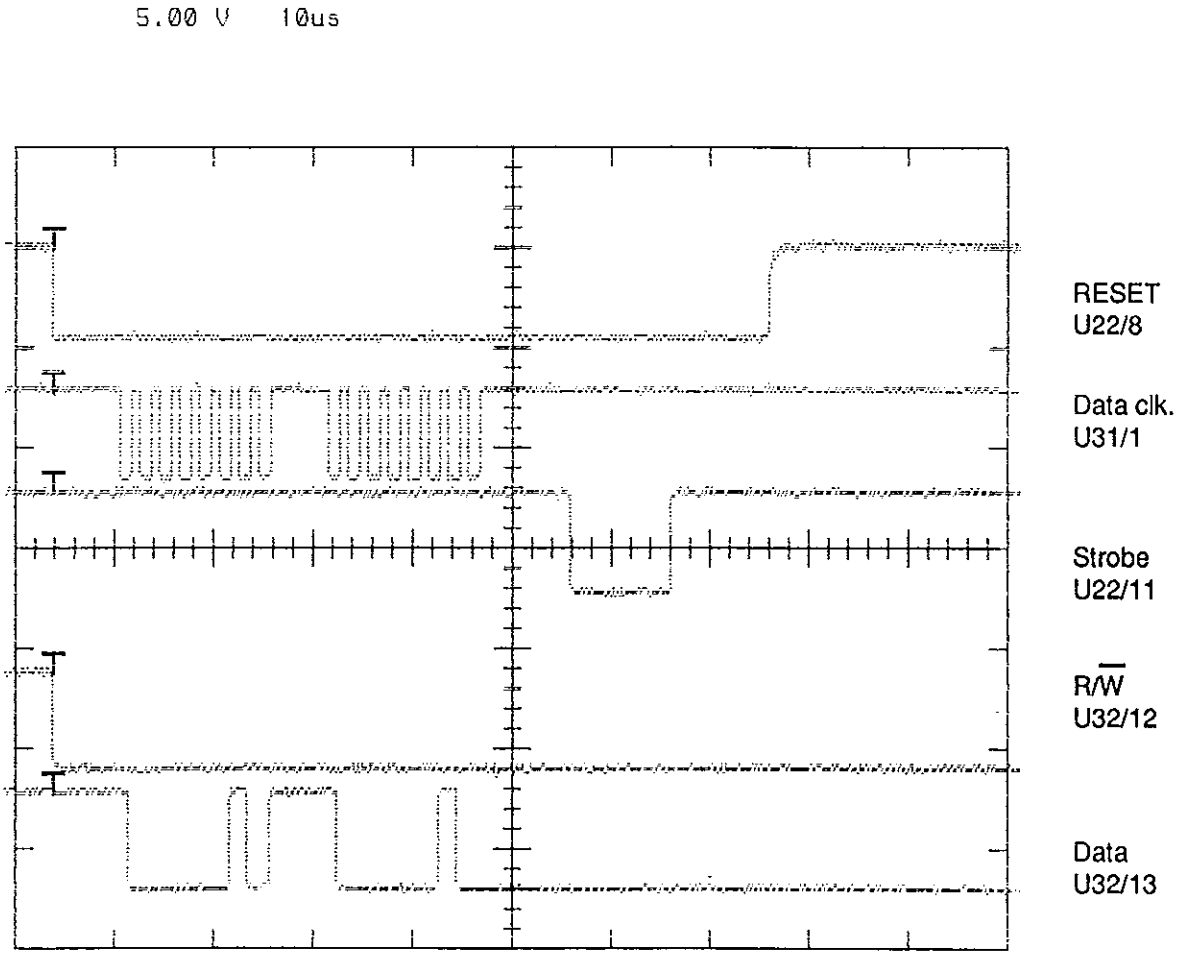

Fig. 7 Digital Output transaction

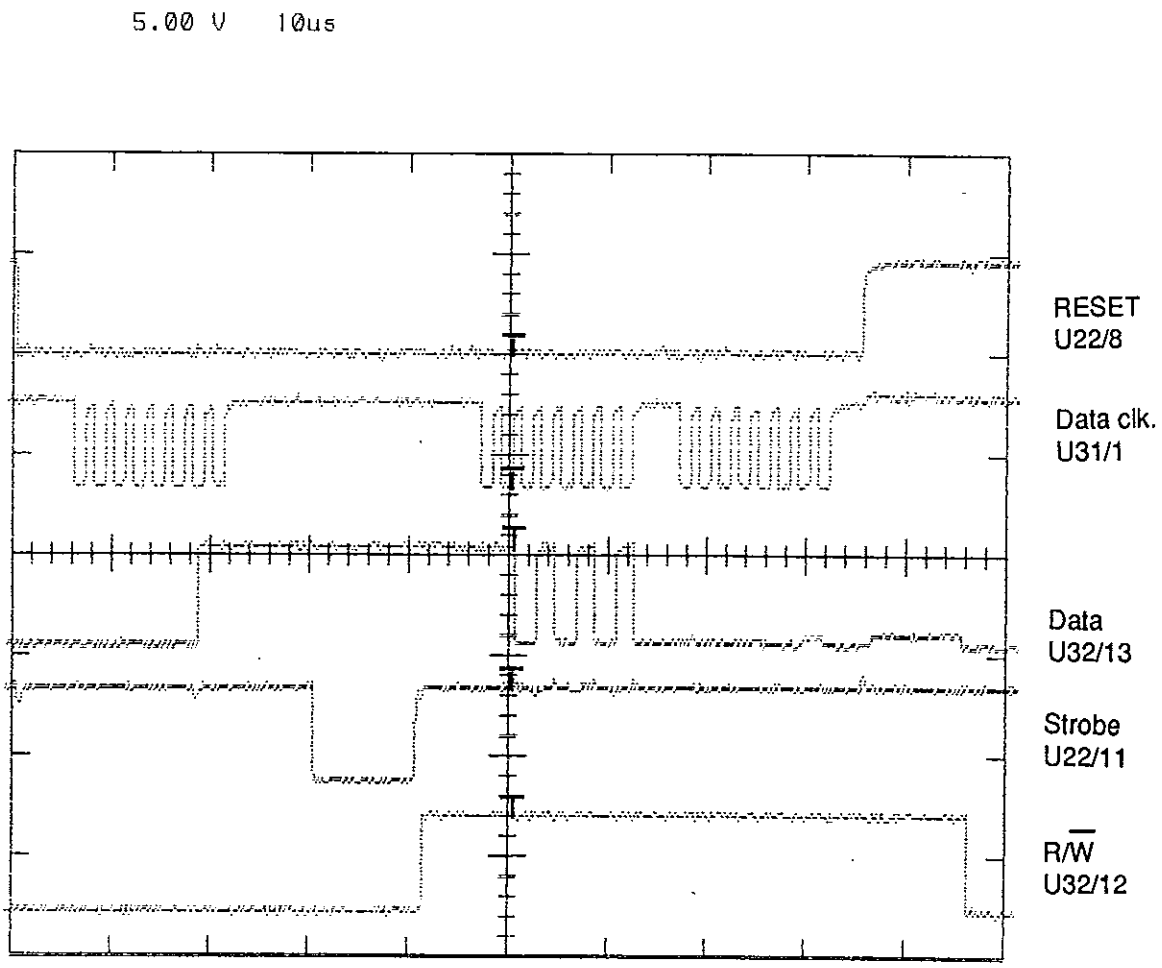

Fig. 8 Digital Input transaction

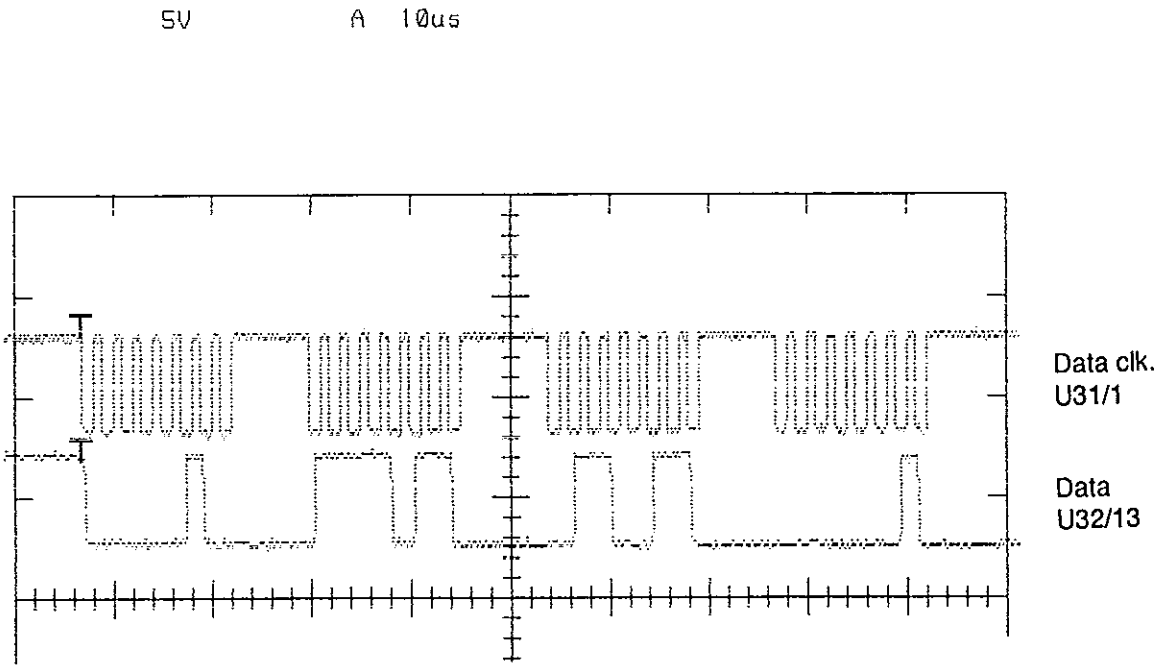

Fig. 9 Analogue Output transaction showing relationship between Data Clock and Data

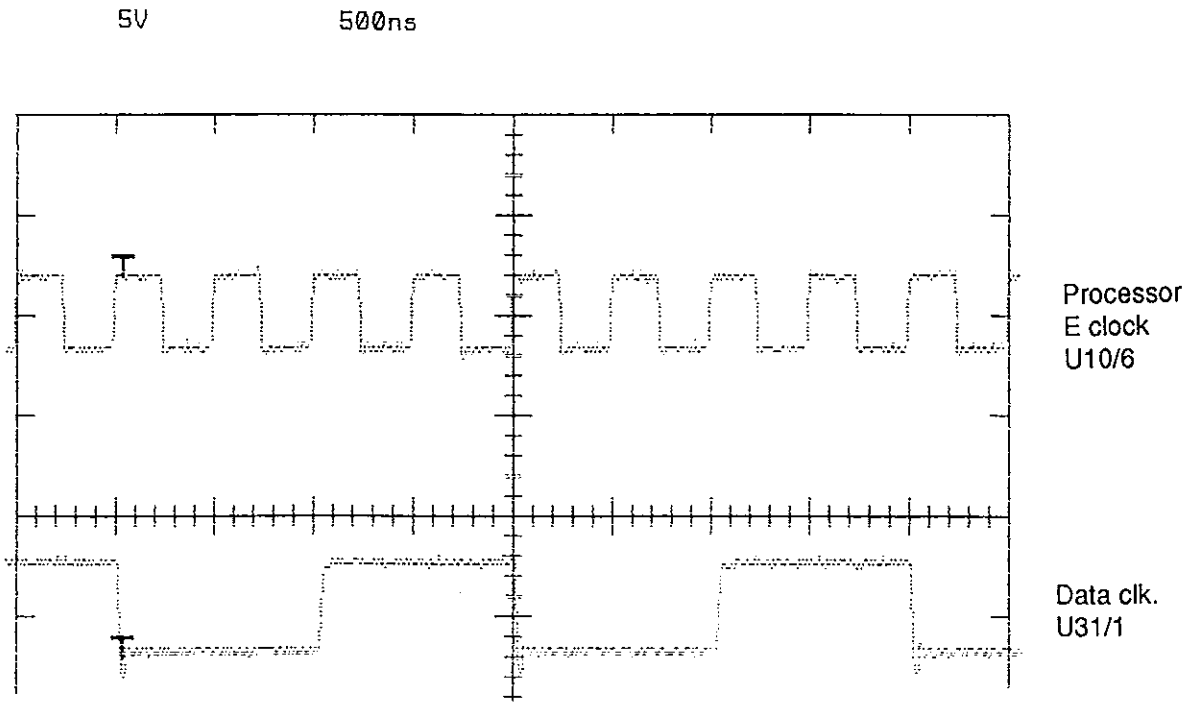

Fig. 10 Relationship between Processor E clock and data clock