Contents Page

Appendices:

Circuit Diagram AI 150050 G
PCB Assembly AH 150050 G

1 General description

The FICS-11 system has been designed so that the operator Panel plays no direct part in the real time control of a FICS-11 system, i.e. the system will continue to run although to panel is defect or disconnected. The Operator Panel is powered by a 38 V supply generated for this purpose only.

An on-board microprocessor with its firmware, userware and working store control the communication to an interface chip in the Main Controller 662 module, the 40 character display and the reaction to operation of the membrance keypads. The microprocessor also drives buffers for the RUN, HOLD, ALARM, NUMBER and ENABLED indicators.

2 Description of circuit elements

Refer to circuit diagram AI 150050 G and PCB layout AH 150050.

2.1 Power Supplies

The incoming voltage, which is used to derive all voltage supply levels within the unit, is arranged to be at 37,5V minimum and 39.5V maximum. The voltage drop in the panel cable between the module rack and the panel depends on the length of cable. The voltage output at the power supply is set to allow a voltage drop in the cable so that the incoming supply voltage at the Operator Panel is within the range required.

The common mode choke L1, C1 and C2 provide incoming interference suppression for the supply and the digital interface signals. Digital communications signals are not degraded by the choke. Q1, Q2 and associated components provide a filter which blocks transients generated by the switching power supply inside the panel from being transmitted back down the ribbon cable. The input of Q1 is about 1V higher than the output of Q1. The output is regulated to 30V by Q6, Q5 (a constant current source) and D13, D14.

5V Supply

This is derived from the output of Q1 via a switch-mode circuit formed by the controller, U1, switching transistors Q3 and Q4, filter components CH1, C19, and C20, and the associated driver, feedback and current sense components.

The 5V output is sensed at pin 1 U1 and compared to a reference voltage, pin 2 U1. The internal circuit provides a switched output, U1 pin 11, whose mark-space ratio varies in proportion to the error signal between pins 1 and 2, of U1. The output switches Q3 and hence Q4 on and off. The switched voltage at the emitter of Q4 is filtered by CH1 and C19 to give a 5V dc output. Z1 prevents the output voltage rising above 5.6V.

Current limiting is achieved by sensing the voltage drop across the parallel resistors R25 to R28. If this voltage is too high the inputs of U1, pins 17 and 18 detect this and reduce the switching output.
Filament supply

This supply is derived from the 5V supply by an overwinding on CH1. During the flyback period the voltage on the overwinding is 10V (due to the turns ratio of the windings). This is rectified and smoothed by D17, C17 and C18 and added to the 5V supply to give a filament supply. R23 limits the inrush current and R24 provides a ballast load.

45V driver supply

The switched output of T4 used to derive the 5V supply is also used to derive the 45V driver supply. Switching transistor Q4, drives a diode pump circuit (a voltage doubler) formed by D19, D20 and C21, C22 the output of which is fed to the collector of Q8, a series regulator, the output of which is nominally 45V. This voltage, however, is varied continuously by the circuit associated with U2 to compensate for brightness along the length of the tube.

2.2 Tube Brightness compensation and Reset Circuits

The tube brightness is proportional to the square of the voltage between the filament and the anode dots. Because the filament voltage varies along the length of the tube some compensation in anode voltage needs to be made. This is done by varying the 45V output voltage.

U2 acts as an integrator whose output voltage will ramp positively. The integrator is referenced to ground by R36 and Q12, which is normally on. The output of U2 is fed to the reference voltage summing point (base of Q10) via R34. The increasing voltage will cause a decreasing voltage at the emitter of Q8.

The integrator is reset when the first character is enabled. At this point a pulse through C26 turns Q11 on and discharges C25 through R38. The effect is to cause the anode voltage to return to its peak value at the beginning of each scan of the display.

Under normal operating conditions the display is scanned regularly, therefore the integrator output will never be allowed to ramp into saturation. If the panel does not, for any reason, update its display, the output of the integrator will ramp beyond about 23 volts at which point the diodes D29, D30 and D31 will conduct and reset the microprocessor via Q13. Q14 plus R66 provide hysteritic action to ensure a clean switch action of the reset signal.

During a panel reset Q12 will turn off which means that R36 will no longer be referenced to 0V, instead R39 in series with R36 will cause the integrator output voltage to ramp down. At this time the current through R40, D26 will hold the reset line low. However, most of the current supplied by R40 flows though the clamping diode D24 into the base of Q10 and this causes the 50V output to drop to a relatively low level. When the voltage at the output drops sufficiently D28 will conduct and starve D26 of current to return high and the panel will have another opportunity of starting up correctly.

The output of Q13 is inverted by one gate of U4, the output pin 6 of which controls the resetting or inhibiting of U5, U36 and U15.

2.3 Bleeper and Baud Rate Oscillator

When the bleeper is enabled it gives an audible acknowledgement when certain keys are pressed or when alarms occur (see the FICS-11 Operator's Manual). The duration of the bleep is determined by the software.and the tone is defined by a timer circuit U8. The bleeper is a.c. coupled to U8 by C30.

The baud rate oscillator is formed by a 4.9152 MHZ crystal connected in the feedback loop of gates U3, the output of which is divided down to 76.8Khz by U5. The output of U5 is fed to pin 10 of the microprocessor.

2.4 Address Decoding

The lower order address lines are obtained by latching the address from the multiplexed data/ address bus using U14. On receipt of an address strobe pulse the address is transferred to the latch outputs. The higher address lines are not multiplexed and come directly from the microprocessor. The highest address bits are decoded for selecting system RAM U20 or one of the three userware chips U17, U18 or U19. Refer to the memory map in Fig.1.

Address bit A15 is used via an inverter in U3 to select the firmware chip U16 which can occupy up to 32KB at the top of the address range. However, U16 will be inhibited by U15 pin11 (Y4) via U3 pin 10 between 8000 and 9FFF so that the useable address range of U16 is from A000 to FFFF.

The versatile interface adaptor U11 is enabled via U4 pin 12 when A13 and A14 is high and A15 is low, i.e. in the range 8000 to 9FFF.

During power-up U15 is disabled by Q20 driven from the +38V via threshold zener diodes D41 and D42 until the 5V voltage rail has stabilized. This is to prevent unwanted "writes" to EEPROM userware (when fitted). C62, C63 and C64 prevent unwanted "writes" to EEPROM (when fitted) during power down.

2.5 Display Tube, Dot and Character Scan

Each individual character consists of 35 dots. The state of each dot is clocked into the shift registers U21, U22, U23, U24 and U25. The output of these registers are latched internally and buffered by the display driver U26, U27, U28, U29 and U30. The purpose of the latch is to hold the character information whilst the next character is being input. This reduces display flicker.

The particular character to be updated is selected by clocking a logical "1" into the shift register U36. This "1" is clocked through U36, U37, U38, U39 and U40 to enable each character in turn as it is updated. Each character is updated every 20ms which is fast enough for the eye not to notice that the display is multiplexed.

2.6 Key scanning

The keys are scanned once every display cycle i.e. every 20mS. There are 4 scan lines and 8 input lines to detect the result. These are PA4 to PA7 (scan, pull downs) and PBO to PB7 (Inputs).

R47 to R54 ensure that the inputs PB0 to PB7 remain high when no keypad is pressed and R55 to R62 together with C33 to C40 afford HF interference suppression for the open membrane contacts across the panel surface. U6 and U7 ensure clean switching of the PB0 to PB7 inputs.

The poll to determine if a keypad is being pressed is started by setting all the scan lines to active low and by reading the 8 inputs. If none of these are set low then no keys are pressed. If an input is found to be low then the scan lines are set low in turn until a particular key which has been pressed is identified. As a check the inverse scan pattern is taken to check that two keys are not pressed at the same time.

2.7 Serial Input/Output

U13 has serial input and output capability. U10 and U9 respectively, are permanently enabled to provide the transmit and receive RS-422 level interface for the transactions to and from the Main Controller. For full details about transactions refer to the Main Controller description.

2.8 LED indicators

The drive signals from the microprocessor outputs at P10 to P14 are inverted by the buffer transistors Q15 to Q19 to drive the LEDs, D43 to D47 visible from the the front through the keypad membrane.

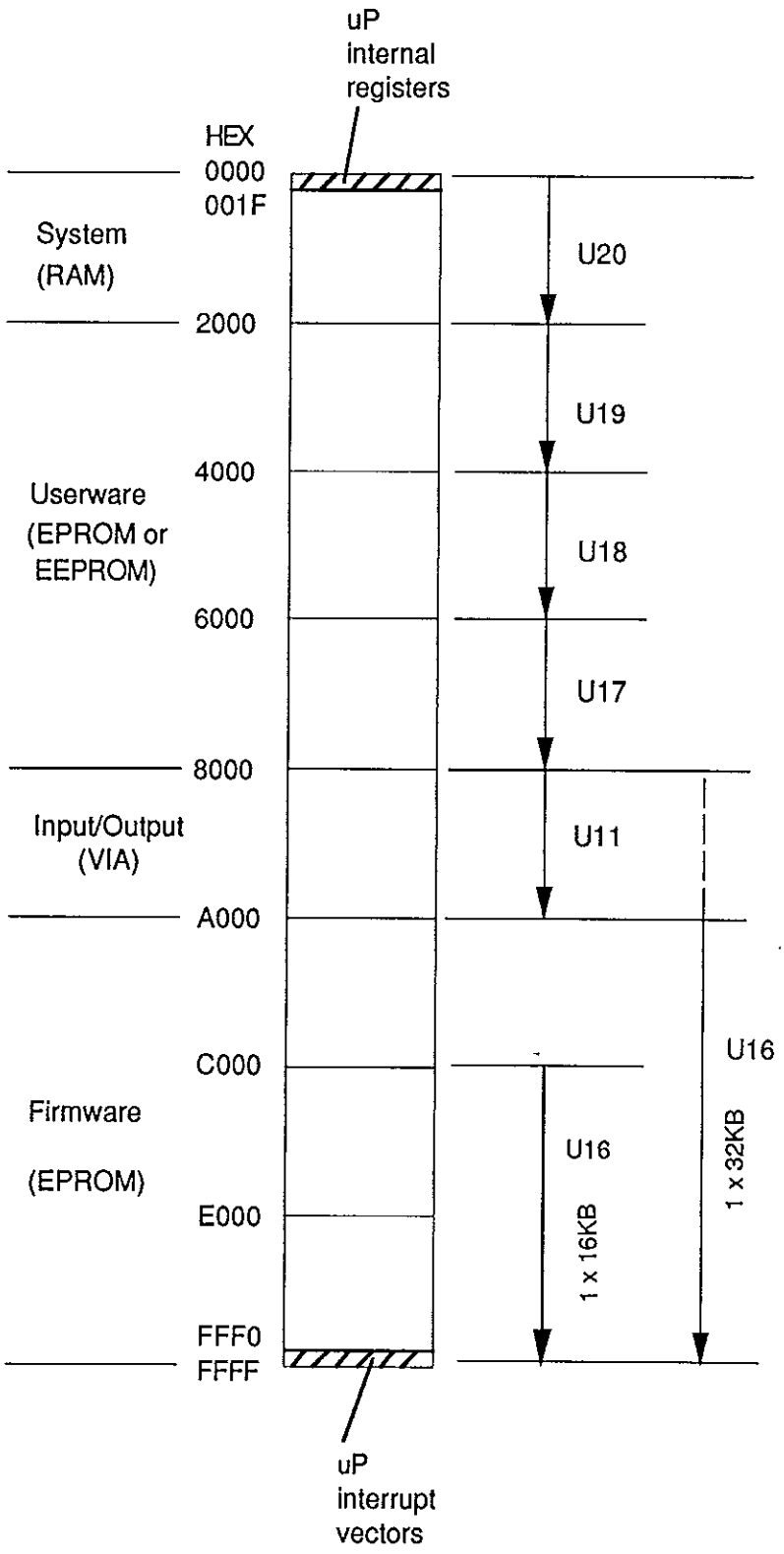

Fig 1. FICS-11 Operator Panel memory map

Contents

Appendices:

Circuit Diagram AI 150051 F
PCB Assembly AH 150051 E

1 Principle of operation

The mains input is interference suppressed and then full wave rectified and smoothed. Three primary switched isolating convertors working off the high voltage DC are used to generate:

+ 5V, +15V -15V from Tr1
+24V from Tr2
+38V from Tr3

The +5V, +24V and +38V rails are regulated via opto-isolator feedback to the primary switch circuitry. The +5V output regulates the voltage on its sense leads which allows accurate control of the +5V at points outside the power supply, i,e. directly at the input to the FICS main controller board. The +15V and -15V rails are regulated by serial integrated circuit regulators on the secondary side.

Current limit for the +5V supply is derived from a primary current measurement which holds back the primary switching control to limit the output with a soft current limit action.

The +15V and-15V currents are limited by the integrated ciruit regulators.

The +24V and +38V currents are limited via the primary switching circuits and have a soft current limit action.

The power fail circuit senses the mains voltage with a rectifying opto-isolator and arranges, via a timer, that the power fail signal switches from an active pull up high to a passive pull down low level a maximum of 13 msec after mains voltage is removed and a minimum of 40 msec under worst case conditions before the +5V output has collapsed by 50mV.

2 Description of circuit elements.

2.1 Input circuit, rectifier, smoother

The mains input voltage is applied first to the 6.3A fuse S1 then to the transient current limiter NTC resistor R2 and to the common mode interference filter Dr1, C2 and C3. C1 provides series mode interference suppression and R1 allows discharge of the input capacitor. R4 is normally not fitted and R3 is a VDR resistor to further protect the full wave rectifier from high energy series mode spikes.

Connector X-1 supplies the mains input voltage via a screened cable to the front double pole mains switch. The output of the mains switch is applied to the full wave rectifier Gr1. C6.1, C6.2, C7.1 and C7.2 smooth the rectified mains signal. R5 and R6 provide discharge paths for C6 and C7 when the supply is switched off and zener diodes D1 and D2 provide transient overvoltage protection of the DC voltage in case too high a voltage is applied to the converter circuits when the wrong mains voltage is applied or the selector switch ST.1 is in the wrong position. Fuse S1 and some other components in the input circuit will blow under these conditions.

C71 decouples the DC supply series switching transients and C4 and C10 provide suppression of common mode switching transients to earth.

Switch ST-1 is the range selector switch which, for the mains voltage range 85 to 132V, connects the neutral end of the supply (X-1 pin 5) to the centre tap of the smoothed DC supply. For this connection C6 and C7 each attain the mains voltage peak and a voltage doubling is effected establishing a DC supply to the converters which is the same at that for the 170...264V supply range when X-1 pin 5 is not connected to the centre tap.

2.2 Mains fail detector

Optoisolator 0C4 is an AC/DC input isolator with a built in full wave rectifier and with a hysteritic switch action. The input current is determined by R67, R68 and P7. R67 is shorted by the second pole of ST-1 for 85...132V mains supply. P7 adjusts the trip point of the mains fail detector so that for voltages at little under 80 V for the lower input voltage range and a little under 160 V for the higher input voltage range the P.F signal will go to zero. This provides extra security for dangerously low mains input voltages. C69 provides a small charge to hold up the internal supply during zero crossover of the rectified input.

The output of 0C4 at pin 6 are pulses switching between +5V and 0V at twice the mains frequency. The pulses are differentiated by C73. The negative pulse cause T12 to conduct and pull IC7 input pins 2 and 6 to +5V. During the time T12 is switched off the voltage at IC7 input decays to about 2V, i.e. still above the trigger input level, before the next negative pulse to T12 pulls the voltage up to +5V again. If the mains supply fails the voltage at IC7 input falls below the 1,67 V trigger level of IC7 and the pin 7 output will go high resetting the PF output to 0V.

The maximum delay between a mains supply failure and the P.F. signal going to zero is 13 msec.

2.3 +5V, +15V, -15V Converter

The converter is of the flyback type where the energy stored in TR1 during the time T1 is switched on is transfered between the primary and secondary when T1 is switched off. Tr1 is not a transformer but, rather, a multiwinding choke. Zener diode D4 provides a switching margin for T1 ensuring that T1 cannot switch large currents until the base voltage has risen to about 4V. C5 and R7 dampen switching spike across T1, C8 holds a charge to ensure that T1 is switches off cleanly and R8 discharges C8 soon aftertion of the voltage induced into winding 6/8 of TR1 ensures that T1 is switched firmly on.

During power up T1 is first caused to conduct by the base current derived from R10 and R14. The primary winding 4/9 and secondary windings 1/2/3 and 10/11/12 have voltages induced into them in reverse to the forward direction of D3, D7, D8 and D11, i.e. no currents flow in these windings with this polarity. The current in the primary winding 5/7 of TR1 flowing through T1 is sensed by the 1 ohm resistor R9. The current will rise until the voltage across R9, which is potentially divided by R11 and R13, cause the switching threshold of T3 to be reached. At this point T3 will conduct shorting the base voltage at T1 to 0V and thus cutting T1 off. When T1 switches off the induced voltages within T1 reverse causing winding 1/2/3 and 10/11/12 to conduct and supply power to the outputs. Windings 5/7 and 6/8 have no current flow (are reversed biased) and winding 4/9 conducts and, although it supplies little power, clamps the voltage of T1 collector to prevent overvoltage. Rectifier/smoother D6, C12 provide a supply for the transistor in opto-isolator OC1.

When the currents in TR1 reach zero the voltages induced in Tr1 will reverse forcing T1 into conduction again. The switching action is self oscillatory and a soft current limit action is ensured via the current sensing action of R9.

The switch off point of TH3 is controlled via feedback from the output transistor of OC1 which is driven from the 5V regulator. The switching frequency varies from about 100 KHZ for no external load to about 25 KHZ for maximum external load.

The voltage from the winding developing the 5,2V output is rectified by D11 and smoothed by C26, C27 and C28. Dr2, C32, C33, Dr3, C35 and C36 further smooth the rectified output.

Control of the voltage at the output sense lines is achieved through IC3, an adjustable shunt regulator in conjunction with the potential divider R28, P3, R29. The voltage at IC3 cathode controls the current passing through the opoi-solator diode of OC1, the collector emitter voltage of its output and hence the primary power via the switch off point of TH3. TR4, T5, T4 and associated components cause R35 and R36 to load the converter when no exterbal load is fitted. This is necessary especially for the double output configuration to make the converter more controllable. TR4 switches T4 off above a small external 5V load.

D12, R22, C29 and Th3 afford overvoltage protection in the event of a defect in the control or switching circuity. D12 is a 5.6V zener diode which causes switch on crowbar action of Th3 for voltages across Th3 of between 6.0 to 6.4V.

R27 and R30 afford default feedback for the sense leads to prevent large devinations from the nominal 5.2V in case an external sense lead is open circuit or when no load is fitted.

D13 and D14 prevent output overvoltage transients when the output power leads are open circuited. D13 and D14 also ensure that when the power supply is plugged in with the mains voltage switched on the transient making and breaking of the power and sense connections do not cause overvoltage transients or overvoltage crowbar action of Th3.

D32 is the front 5V indicator and C34 decouples common mode switching transients to ground.

The outputs from the centre tapped winding developing the +15V and -15V are rectified by D7, C15 and D8, C16. R15, C13 and R16, C14 are normally not fitted but are provisioned for protection of D7 and D8 for certain types of alternative diodes. Adjustables series regulators IC1 and IC2 control the +15V and -15V outputs via the potential divider feedback circuits R18, P1, R19 and R20, P2 and R21 respectively. D9, R25, C24, Th1 and D10, R26, C25 and Th2 provide crowbar overvoltage protection of the +15V and -15V outputs.

R82 and R83 provide a light internal loading when the outputs are not loaded externally and C22 and C23 filter the output high frequency ripple components. D31 and D30 are the front facia +15V and -15V indicators. C19, C20 and C21 decouple the common mode switching transients to ground.

2.4 24V Converter

The 24V converter is a buck converter and TR2 has true transformer action transferring power to the secondary circuit when the switching drive transistor is switches on. The converter works with a fixed frequency of about 100 Khz. T7 is driven from a pulse width modulated (PWM) driver which is controlled from the feedback of the output voltage via 0C2.

The working principle of the controller REG-1-S can be seen from block diagramm HJ 150051D. Shut down action is not required here and pin 12 is connected to 0V. After switch on R38 and T6 supply REG-1-S with power transiently to pin 9 for a short time until the winding 8/9 of TR2 has had time to build up the supply to pin 10 via the rectifier smoother D16, R81, C42. T6 switches off shortly after power up. After switch on the PWM is inhibited until time out of a short delay, the delay being determined by capacitor C40.

Winding 5/7 of TR2 provides a demagnetising voltage clamp when T7 switches off. Primary current in winding 6/11 of TR2 is sensed by R41 and R42 and fed back to the controller REG-1-S pin 3 after being rectified and smoothed by D19, C41 and C72.

The normally soft current limit action is made sharper by T13 and its associated components. The added current limit feedback from T13 collector ensures thatn current limit of the output starts at around 2.6A and is fully limited to about 3A max., i.e. will not damage the flat band cable carrying the 24V.

The secondary voltage for the 24 V output is rectified and smoothied by the series diode of the diode pair D22, Dr4, C52 and C53.

R53 and C55 quench switching spikes on the secondary winding and the parallel diode of D22 conducts the current in Dr4 during the time that the serial part of D22 is reverse biased.

Th4 provides crowbar action overvoltage control. Th4 conducts when the voltage output reaches a level between 26V and 27V. The switch point is determined by the breakdown of IC4 configured as an adjustable precision zener diode. The breakdown voltage of IC4 is adjusted with P4.

Control of the output voltage is achieved by the shunt regulator IC5 controlling the input current of 0C2. The output voltage is adjusted with P5.

C46 is a high frequency decoupler for the output voltages and C50 and C54 decouple common mode switching transients to ground.

R51 and R52 provide a light load for when the output has no external load. D21 is the front facia +24V indicator.

2.5 38V Converter

This converter works on the fly back principle and the primary side works in the same way as the 5V converter described above. Here instead of a thyristor being used to cut off the conduction of the drive transistor T8 a double transistor switch T9, T10 is used. Control is also achieved in the same manner via IC6 its associated components and 0C3.

The 38V output is isolated from other outputs and is derived from the rectifier D27, C64, C65. The output is controlled by the shunt regulator IC6 which controls the output current via the input current of 0C3. P6 sets the output voltage. D28 is the front facia 38V indicator.

The +38V is used to supply the FICS panel only and does not require overvoltage protection as the panel circuitry contains further voltage regulators.