EUROTHERM

Maintenance Manual

Controller/ Programmer Type 815/818

RECORD OF AMENDMENTS

Amendment No.	Date	Pages Effected
1	1 June 1988	Cover Title page Record of Amendments page Contents list Data Sheets Installation Instructions Operating Instructions Chap 22.3 Addresses
2	22 September 1989	All pages individually identified Chapters re-arranged and updated to current instruments state Dallas Non-Vol RAM and Valve Positioner information incorporated
3	30 January 1990	Record of Amendments page Chap 5.0 Contents Page Chap 5.0 Pages 13 to 18 Addresses

815/818 MAINTENANCE MANUAL

CONTENTS

Chapter 1.0 **General Description**

Contents

1.0 General Description

1.1 815/818 Programmers/Controllers

The 818/815 controller is a three term controller with a heat channel output and an optional cool channel. A maximum of two alarms can also be fitted. If only one alarm output is required on model 818 the other output can be configured as a retransmission signal. Alternatively, if the cool channel is not required this can be configured as a retransmission signal. Either or both of the alarm outputs can, if not required as alarms or retransmission, be configured as programmer segment driven outputs on model 818P or 815P only. The valve positioner version of the 818 controller can only have one alarm driving a relay when a feedback potentiometer is incorporated. A remote input (3) can be fitted to channel 4 as an option in place of the alarm 2.

Summary of Control Outputs - Retransmission Outputs
Analogue Inputs (818 only)

Slot	Location	Prime Function	Aux Function
Channel 1	PSU	Output 1	
Channel 2	Options Bd	Output 2	Retrans (1)
Channel 3	Options Bd	Alarm 1	Retrans (2) or Program segment drive
Channel 4	Options Bd	Alarm 2	Remote input (3) or Program segment drive

(1) Possible if no Analogue Comms fitted and a DC output installed, and instrument configured as Heat Only.
(2) Possible if no Analogue Comms fitted, and Alarm 1 configured with a DC output installed.
(3) Possible if no Analogue Comms fitted and Alarm 2 configured with an input module fitted.

The signal input can be configured for thermocouple, RTD, voltage or current inputs. On model 818 it is also possible to configure the input for a pyrometer. The model 818 single FIP display carries two five digit 7 segment displays plus a single digit 7 segment display plus various other legends. The F.I.P. on the model 815 carries a single 4 digit 7 segment plus error bar display plus various other legends. The instrument functions are operated by a total of six push buttons mounted on the front of the controller.

Instrument voltage supplies are provided by a switch mode power supply. Each of the alarm and output stages are in a modular printed circuit board form. These boards plug onto pins on the power supply and options board.

A single Intel microproccesor type 8032 drives the controller, display and communications facilities, if fitted. (See figure 1).

It is recommended that servicing of the instrument is only carried out to board level. Once the faulty PCB has been located this can be returned to your nearest Eurotherm office, refer to back page for addresses, where a serviceable exchanged board is available. To assist in this diagnostic procedure or if it is required to service down to component level then a set of extender cables,will be found to be very useful. These extender cables allow the daughter boards to operate remote from the display board. It may also be useful to use the individual rear terminal block, for making connections to the rear terminals.

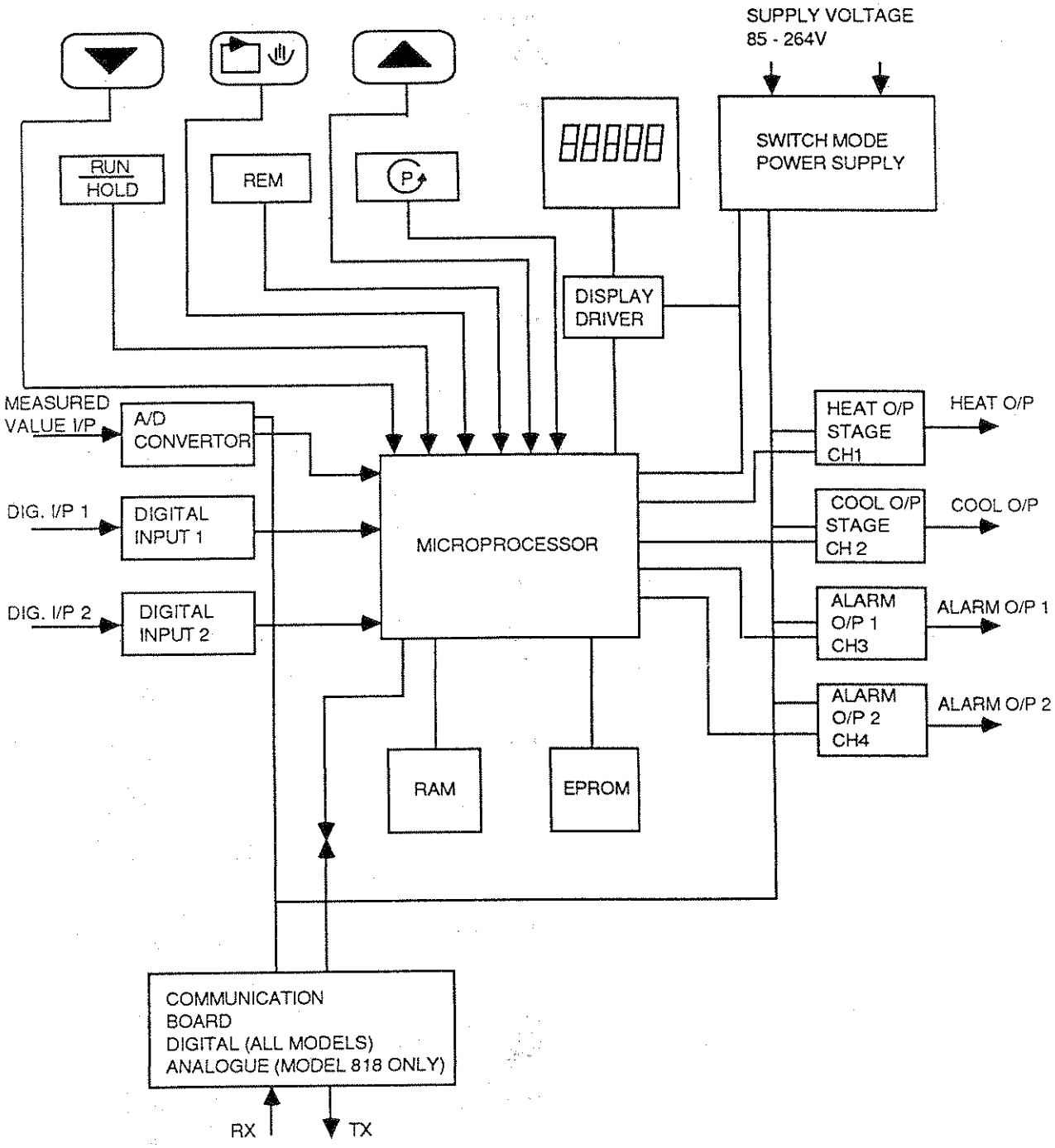

Figure 1. 818 Schematic Diagram

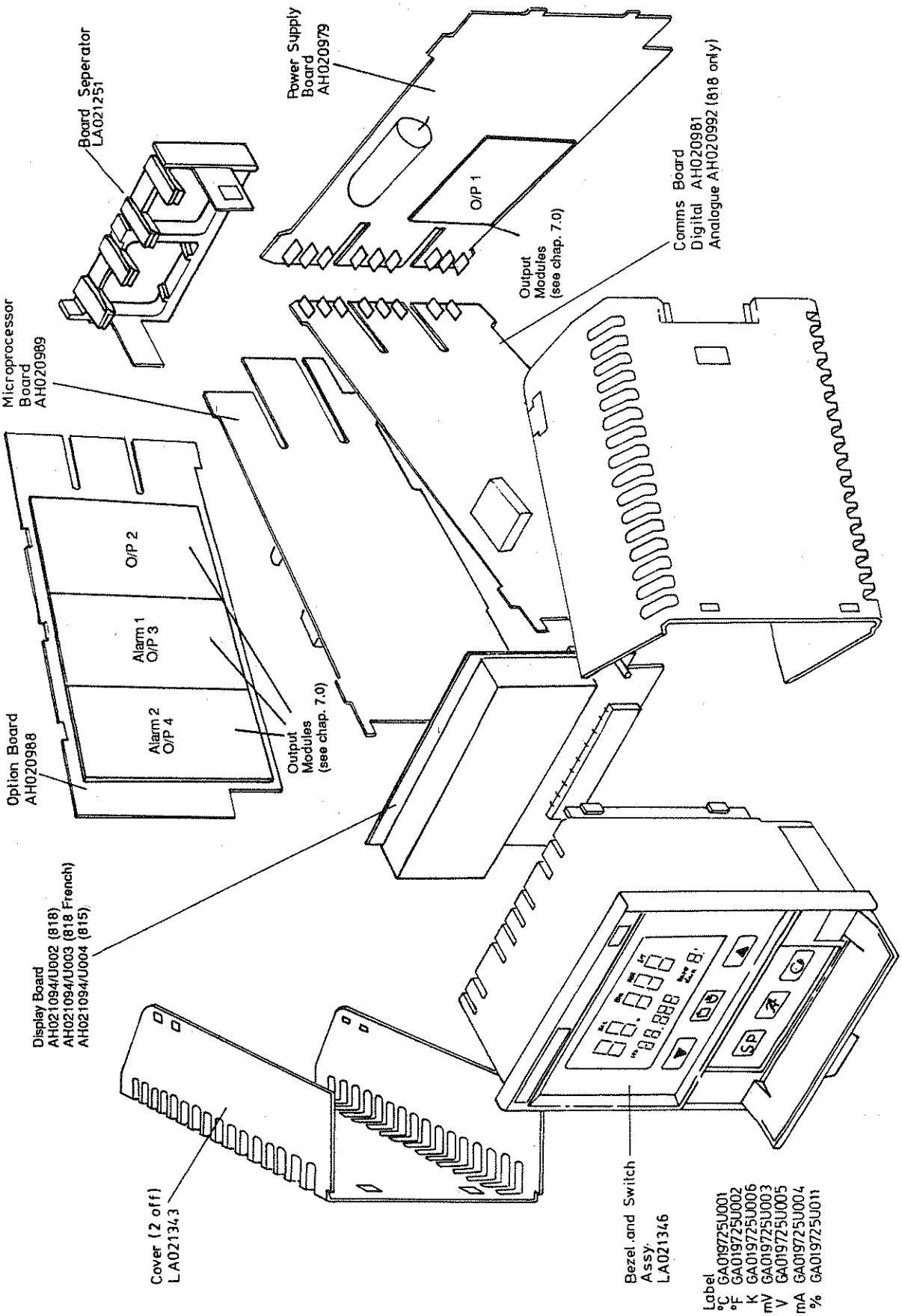

Figure 2. 815/818 Exploded View

Chapter 2.0 **Dismantling the 815/818 Instrument**

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2.0 Dismantling the 815/818 Instrument

2.1 Dismantling Procedure

Remove the instrument from its sleeve by turning the locking screw, in the lower right hand corner of the front bezel, in an anti-clockwise direction until a stop is felt. The instrument will now be ejected from the sleeve connections and withdrawn by pulling out of the sleeve.

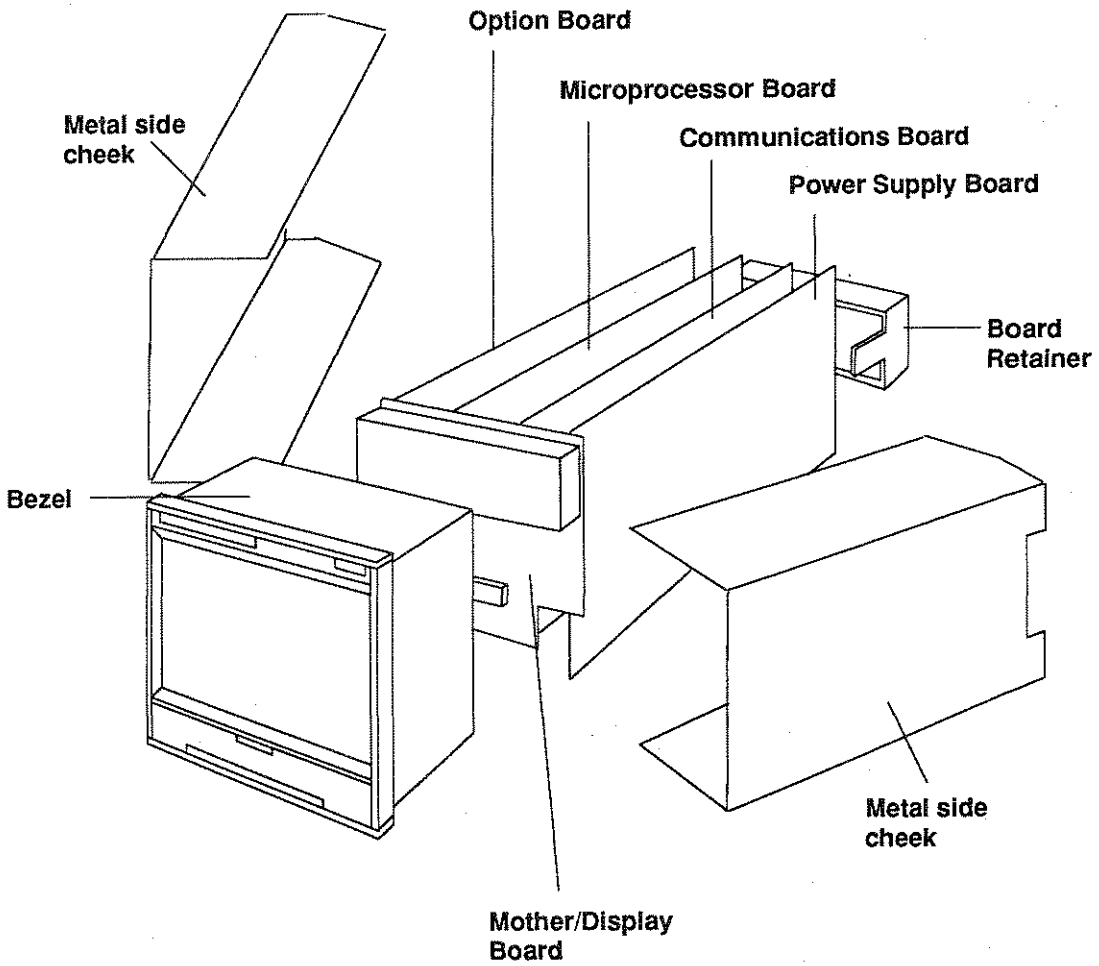
The catches of the board retainer can now be released by inserting a screwdriver into the slot in the square cut-out on each side of the instrument, pushing the retainer into the centre of the controller and then push towards the rear of the instrument. Once this retainer has been released from both sides of the instrument it can be withdrawn from the rear of the instrument by pulling by hand. Note, this retaining strap is handed and must be reassembled the correct way, ie, with the metal clips on the retaining strips in line with the metal connectors on the boards.

With the board retainer removed the metal side cheeks of the instrument can be removed by hinging them down about the edge nearest the instrument bezel.

The printed circuit boards can then be unplugged from the mother/display board by pulling them away from the bezel. When removing the last board it may be necessary to retain the mother board in the bezel.

Before removing the mother/display board from the bezel the flexible printed circuit from the push buttons must be removed from its connector. This can be achieved by gripping either end of the connector and pulling away from the printed circuit board. The central part of the moulded connector will slide back to a stop position which will release the flexible printed circuit which can then be carefully removed from the connector.

To reassemble the unit carry out the above procedure in reverse, ensuring that the bright metal strip on the side cheeks are positioned at the bottom of the instrument.



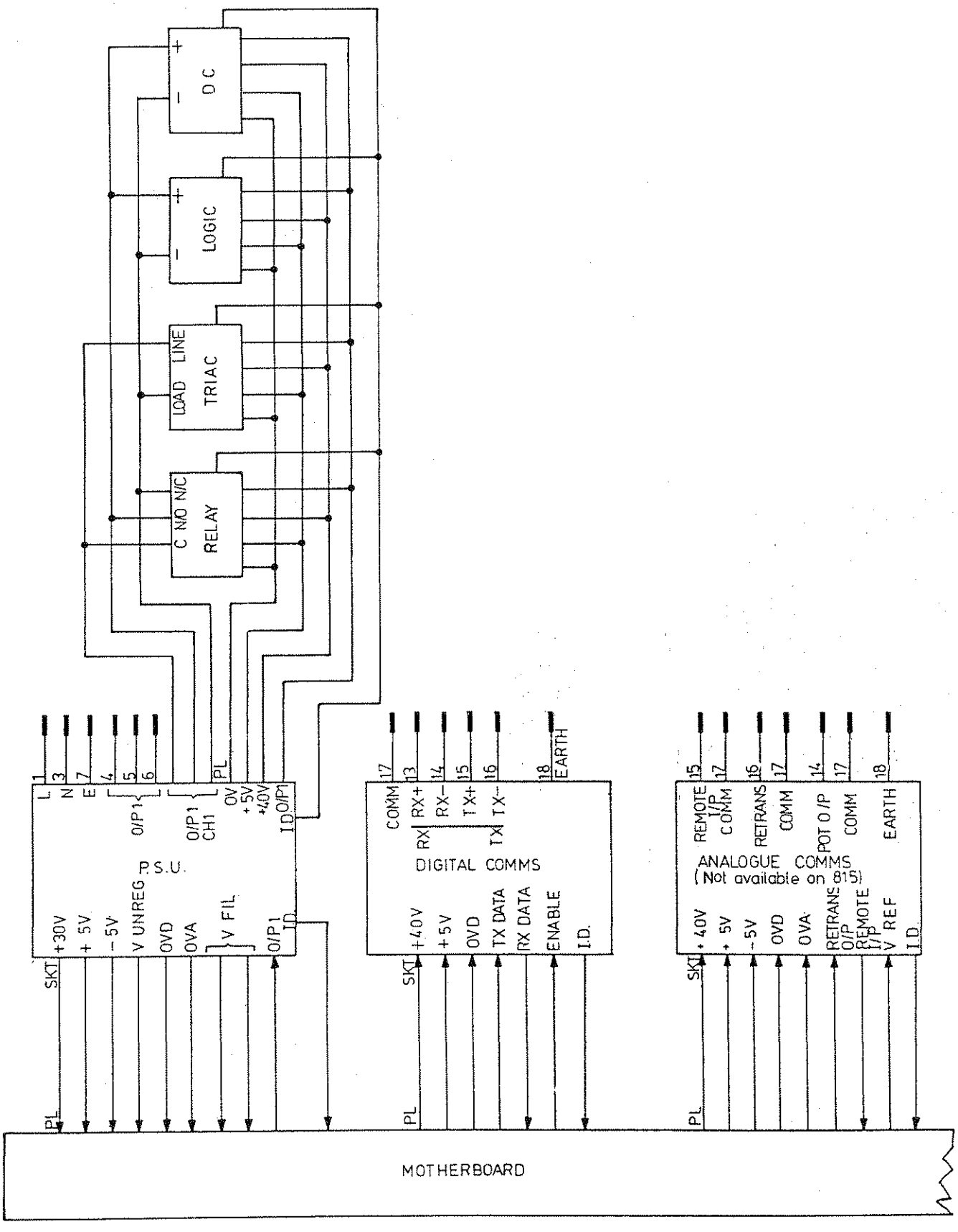


Figure 1a. Board Interconnection Diagram

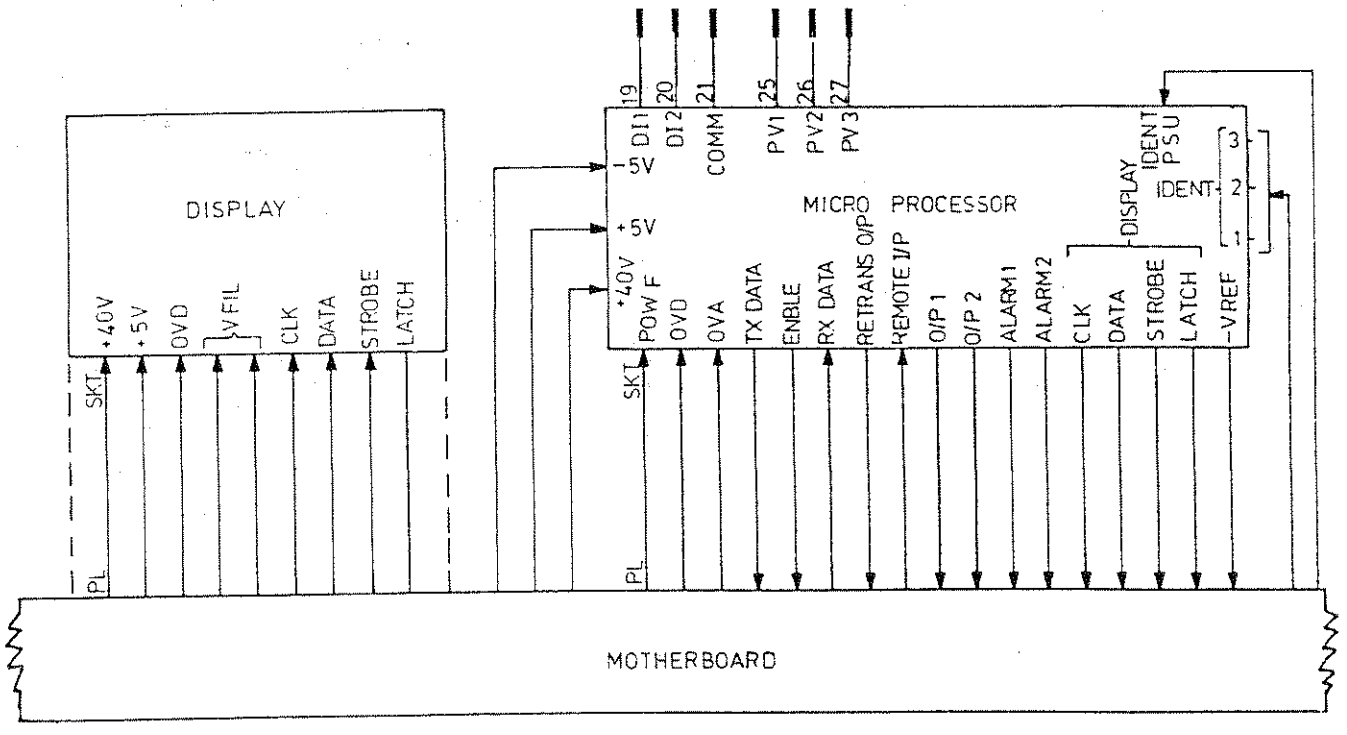


Figure 1b. Board Interconnection Diagram

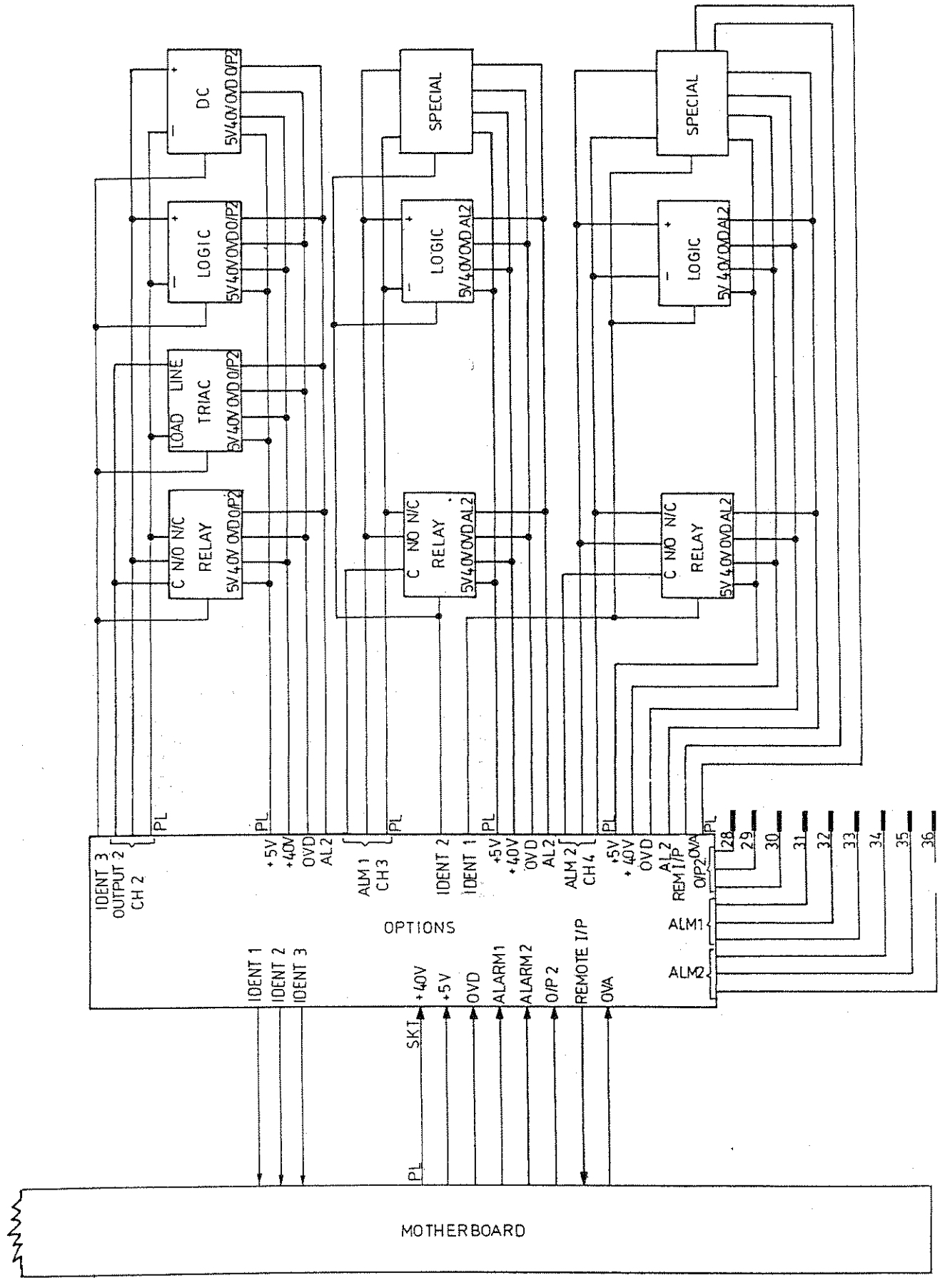


Figure 1c. Board Interconnection Diagram

Chapter 3.0 **Power Supply**

Contents

3.0 Power Supply Board

3.1 Specifications

Operating temperature range 0-70°C

Board : AH020979 (Standard)
AH022076 (Low Voltage)/Standard from September '89
AH021520 (CNOMO)

INPUT Standard : 85 to 264 Vac)
@ 48 to 62 Hz

Low voltage 18 to 40 VAC @ 48 to 62Hz)
or 20-40Vdc

OUTPUT :	5V +/- 10% @ 100 to 200mA	Ripple	100mV max
	40V +15%- 5% @ 15 to 150mA	Ripple	1V max
	-5V +/- 4% @ 5 to 30mA	Ripple	50mV max
	2.8V +/- 10% @ 240 to 300mA	Ripple	300mV max

Typical power consumption 10 watts (15VA max.)

There are three versions of this board.
Adjustment potentiometers are not fitted into any of these units. For this reason there is no setting up procedure. Most versions are also not fitted with any links.

The 'CNOMO' board AH021520 does have links to select one of the two output stages installed upon it. Links are also fitted on to the board for selecting either a voltage or current output and for placing the snubber network across the normally open or normally closed relay contacts.

3.2 Introduction

There are three versions of the power supply board, standard, low voltage and 'CNOMO".
Most instruments, either 815 or 818, are fitted with a standard power supply the circuit being shown in figure 3 and the layout figure 2.
The low voltage version is installed in either an 815 or 818, when it is required to power the instrument from a low voltage, either 18 to 40 volt ac 48-62Hz or 20-40 volts dc. The circuit diagram is shown in figures 5 & 6 and the layout in figure 4.
The third option is the CNOMO power supply board. This has a standard high voltage power supply end but has two alternative heat output stages tracked onto the basic board. These give either relay or dc outputs. The circuit diagram of the board is given in figures 9, 10 & 11, with the layouts in figures 7 & 8.

The incoming supply voltage is fused and then filtered and rectified to charge the reservoir capacitor C10 or C9. Current from this capacitor flows through the transformer primary (T1) and the current limit resistor R14 or R15 is switched by Q2. The switched current and voltage waveform being shown on the block diagram.

The drive for the switch is derived from U1, which is initially powered direct from the reservoir capacitor, through the start up circuit Q1 (or Q3) and associated components. Once oscillations have been established, U1 is powered by secondary (2,3) of TI which is recitified and smoothed by D2, C6. The output of secondary (2,3) also disables the 'start up' circuit and is used to provide the voltage feedback to compare with the reference voltage within U1.

Rectification of the secondary is achieved with diodes which are placed in such a direction as to half wave rectify the output during the fly back period.

The voltage across R14 or R15 is fed back into U1 as a current limit signal and is used to keep the current through the primary below a specified level. If a short circuit exists across a secondary winding then the voltage across secondary (2,3) will be dropped to zero and the supply voltage to U1 will decay as capacitor C6 discharges. When the voltage across C6 reaches 10 volts the start up circuit will again be enabled, the drive to the switch Q2 or (Q3) will be disabled and C6 will change until it reaches 16 volts when the start up circuit will again be disabled, once more causing the voltage to drop to 10 volts with Q2 (or Q3) enabled. This form of operation will continue whilst the short exists on the secondary.

This form of operation is shown in the diagram below.

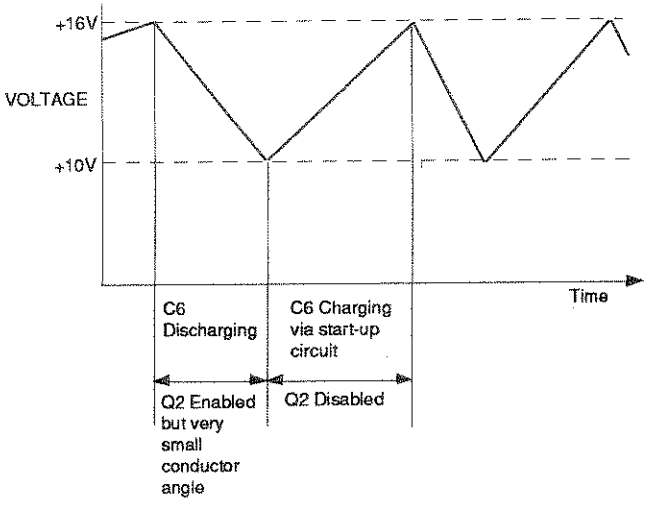


Diagram of C6 voltage during time that high speed current limit is working into a short circuit.

3.3 General

The standard 818/815 PSU board comprises an 'off-line' switched mode power supply unit (SMPSU) and an output 'site' for output 1 which may be fitted with one of four output option types. Only the operation of the power supply will be considered here.

The power supply is based on the 'flyback' principle and derives its input voltage from the rectified mains input, hence the description 'off-line'. The term 'flyback' is used to describe a mode of operation whereby energy is drawn from the input reservoir capacitors and stored in the transformer's primary inductance during the switching elements 'on' time and transferred to the output circuit during the 'off' or flyback period. When the switch is turned off, the current built up in the primary collapses and the voltage developed across the winding reverses or 'flies back' to a voltage determined by the turns ratio of the transformer and therefore, the output voltage. Energy is transformed to the outputs in a repetitive 'change-dump-change' fashion. In this PSU a 'discontinuous' transfer scheme has been chosen mainly on the grounds of smaller transformer. The term discontinuous indicates that the total energy requirement of the load is stored in the transformer each cycle and surrendered completely to the load before the start of the next cycle.

The PSU is intended to operate over an input voltage range of 85-264V ac.

3.4 Input Filter and Rectification

The mains input to the PSU is applied via a 500mA or a 1.25A anti-surge fuse, F1. A bifilar-wound choke, L1 is provided to filter both incoming noise caused by switching of inductive loads etc, and to reduce the levels of conducted common mode signals produced by the PSU to acceptable levels. Other components in the filter include C3, 4 and 5 and chokes L_2 and L_3. The latter serve double duty as inrush current limiters to prevent fuse and rectifier rupture when the power is first applied with input reservoir capacitor, C10 or C9, fully discharged, due to the high dc resistance exhibited by these chokes.

The mains input is rectified by diode bridge, D1 or D3, and smoothed by the electrolytic capacitor, C10 or C9, to produce a dc voltage in the range 100 to 373V. Both 0V and HT star points are employed to minimise problems caused by signals with high rates of change. A disc ceramic, C18 or C17, bypasses the supply directly between the star point.

3.5 Start up Circuit

Prior to PSU start up, current for the control circuit is provided from the HT line by the current source formed by transistor, Q1, zener diode D8 and resistors R6, R8 and R9 or R6, R23, Q3 or Q1, Q4, R8, R9, R10, R49 and R50. The control circuit, UC3842, contains an undervoltage lockout which ensures that all internal functions remain off until the supply pin, pin 7, reaches 16V. This ensures that no attempt is made to drive the MOSFET switch with any voltage less than would guarantee full switching and thereby preventing damage due to overheating. During this phase the current drawn by the UC3842 is 1mA maximum. The combination of D8 and D9 or Q3 or Q11, provides a current of approximately 1.5mA. This current charges the 47µF capacitor, C6, to the required 16V threshold. When the threshold is reached the UC3842 starts to drive the VMOS FET and the output capacitors begin to charge.
Following start up the current source is redundant and would dissipate about 0.6W at high mains. For this reason additional circuitry has been added to turn the circuit off in the high voltage version once the supply is running. A capacitor, C16 and resistor, R13 or R12 ac couple the voltage appearing on the auxiliary winding of the main transformer and diode D12 or D8 clamps this pulse train to the primary 0V rail. This is then peak rectified and smoothed by D11 and C14 to produce a voltage which sits on top of the UC3842 supply rail. This ensures that diode D9 or transistor Q11 becomes forward biased thereby turning off Q1. Diode D10 prevents the current during start up from charging C14. Capacitor C16 is selected to pass sufficient current to turn off Q1 at 85-90V input. Dissipation is negligible under these conditions.

3.6 Control Circuit

The UC3842 is a current mode PWM controller and comprises an error amplifier, current comparator, R-C oscillator and an output driver capable of driving MOSFET's directly. Power is supplied via the auxiliary winding, diode, D2 and resistor, R4 or R5. R4 or R5 is included to prevent the leakage inductance spike associated with this winding from 'pumping up' the capacitor C6. Feedback is also derived from this winding via a separate R-C filter, R1, C1 which again reduces the effect of the commutation spike, diode D1 and capacitor C2. The resistor chain R2, R3 and R17 on R4 set the voltage at the cathode of D1 to approximately 15.7v. All other secondaries produce outputs relative to this. The voltage at the input to the error amplifier, pin 2, is compared with an internal 2.5V reference and feedback ensures that the voltage on D1 is maintained constant. The error amplifier gain is set by R5 or R6. Capacitor C8 rolls off the error amplifer gain above 2kHz.

Resistor R7 and capacitor C12 or C4 set the oscillator frequency to approximately 50kHz.

Cycle-by-cycle current limiting is provided by monitoring the voltage across the current sense resistor, R14 or R15. A small spike filter removes a leading edge spike caused by diode hole storage or stray capacitance effects and prevents premature turn off.

The UC3842 can source and sink 200mA and drives the gate of the MOSFET directly. A resistor, R10 or R13 is included to damp out any parasitic oscillations caused by the tank circuit formed by the gate circuit. The MOSFET, Q2, is an 800V, 8R device.

An energy absorb network, formed by D14 or D9, C15 and R12 or R11 absorbs the energy associated with the leakage inductance of the transformer.

3.7 Output Circuits

The 5V output is rectified by Schottkey diode, D15 or D10 and smoothed by capacitors C20 and C22 or C21 and C25. Capacitor C20 or C21 is a low ESR type selected for low ripple voltage. A small RC snubber is included to damp out ringing during the reverse bias condition and to ensure that the reverse voltage remains below 40V. Schottkey diodes exhibit higher capacitance than epitaxial glass bead types and this tends to resonate with the leakage inductance of the 5V secondary. Schottkey diodes are also very sensitive to even very short duration spikes which exceed the reverse breakdown voltage. Zener, D22 or D16 provides simple overvoltage protection.

A 79L05 regulator, U2 is employed on the -5V output, to ensure that this rail is insensitive to load changes on other rails (cross-regulation effects). Rectification and smoothing is provided by D16 or D11, C21, C24 or C20 and C22 and C27.

The 40V secondary is rectified by diode D18 or D13, BYU27-200 and filtered by C23 and C25 or C29 on C24. A 4R7 resistor, R20 or R19, is connected in series with this output to provide short circuit protection. THIS RESISTOR IS CRITICAL AND SHOULD NOT BE REMOVED.

The final output is a 2.8V output for the FIP filament supply. Again a Schottkey diode, D20 or D14 is employed. A 6V 'grid out off' voltage is created by zener, D21 or D15.

An unregulated rail, POWERF, is provided by D17 or D12, R15 or R16 and C26. This rail represents the voltage on the HT capacitor, C10 or C9, and is used for power fail and power feedback purposes. R15 or R16 reduces the effect of short duration commutation spikes and prevents peak rectification by D17 or D12, C26.

3.8 Short Circuit Protection

In the event of a short circuit on any output, the operation of the supply becomes audible since although operation continues at 50kHz, the effect of capacitor C6 being continuously charged and discharged reduces the repetition frequency. Actual repetition frequency is slightly line voltage dependent. Operation is as follows: When an output is shorted all outputs collapse since the voltage during the flyback period is reduced to a low value.

Thus insufficient voltage is available to support the UC3842 and capacitor C6 is rapidly discharged towards the UC3842s lower threshold of 10V. When this level is reached the supply turns off and C6 is charged to 16V via the 1.5mA current source. The supply switches on and operation continues until the current drawn by the UC3842 once again discharges the capacitor to 10V. Operation continues ad infinitum. Since the PSU operates in fixed frequency mode, in the event of a short circuit, the current in the primary must decay sufficiently during the off period so that 'staircasing' and eventual saturation does not occur. It has been found that in order to ensure sufficient discharge in the event of 40V short circuits, some series resistance is necessary to achieve this. Load regulation is affected slightly.

For functional descriptions of the Cnomo power supply board, AI021520, see this chapter, and for Cnomo outputs see chapter 7, relay and DC outputs, as these are functionaly equivalent.

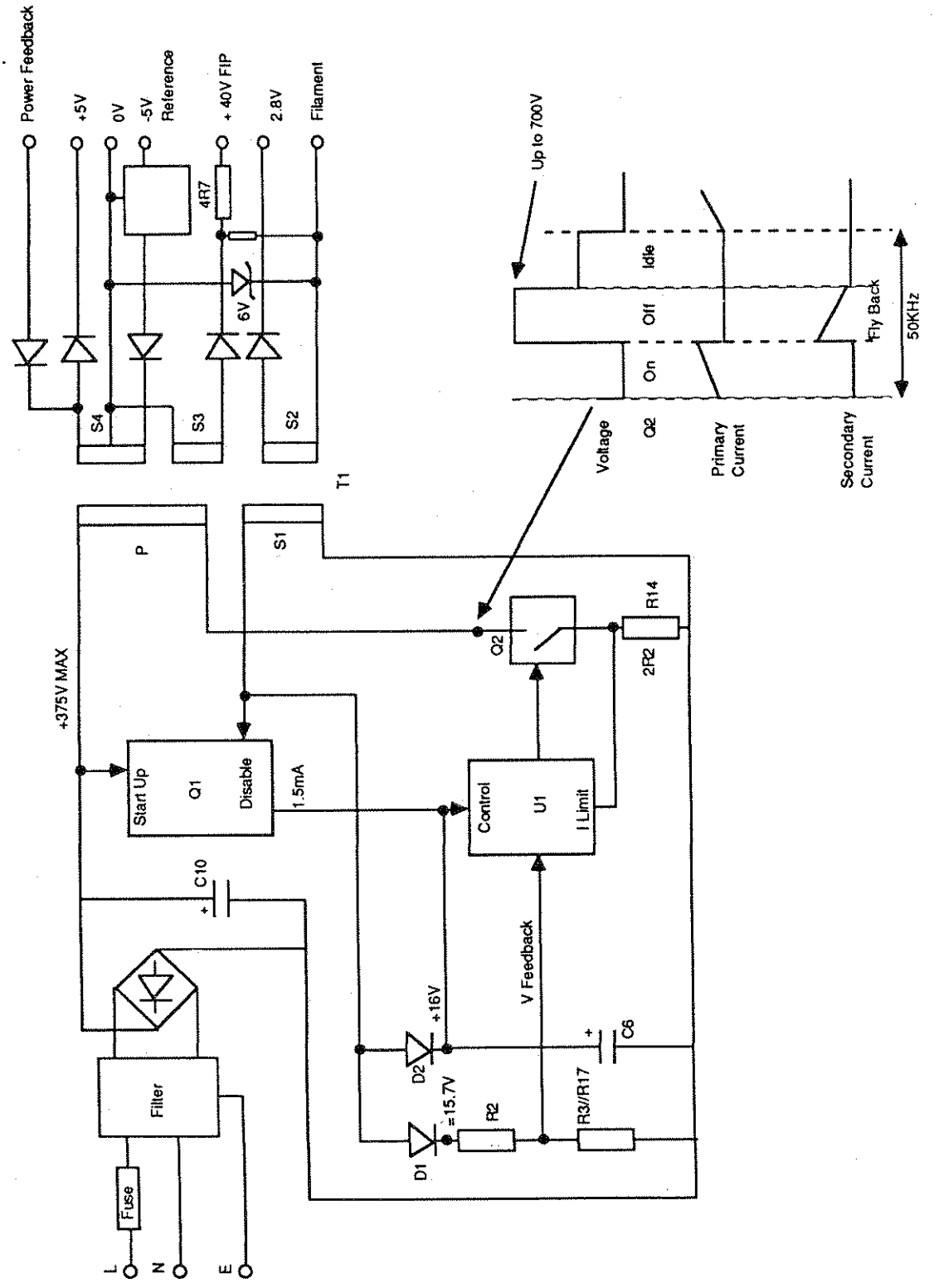


Figure 1. Power Supply Block Diagram

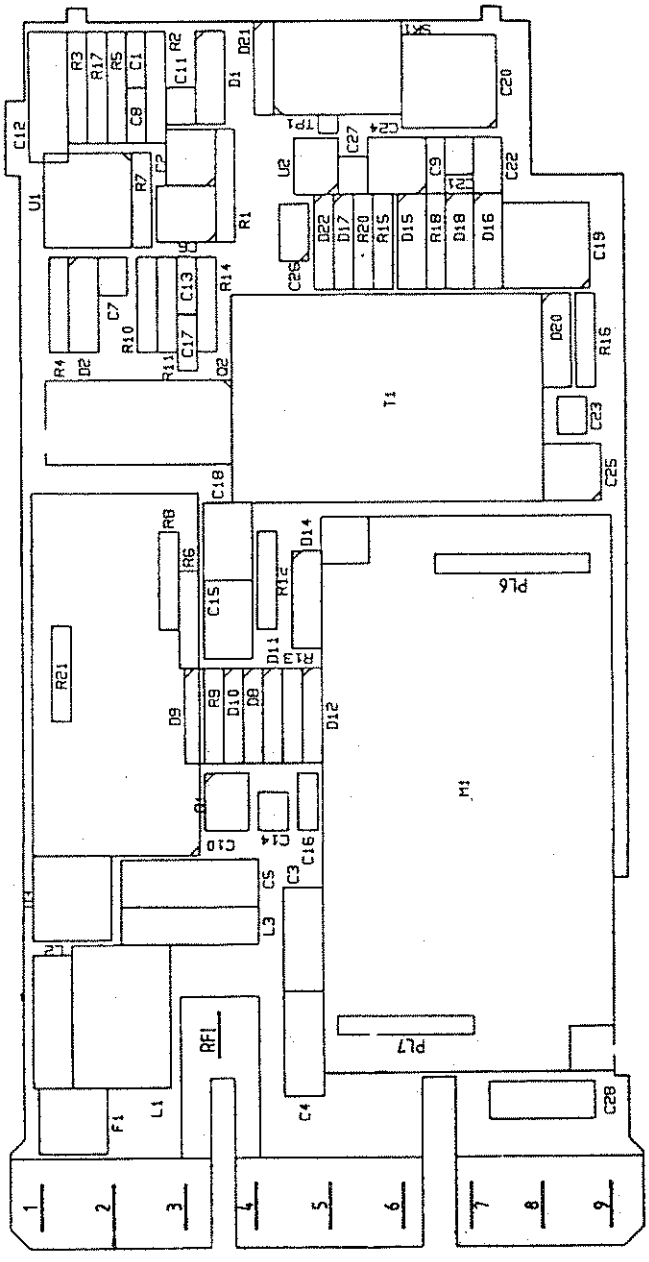


Figure 2. Power Supply Layout AH020979 Iss 1

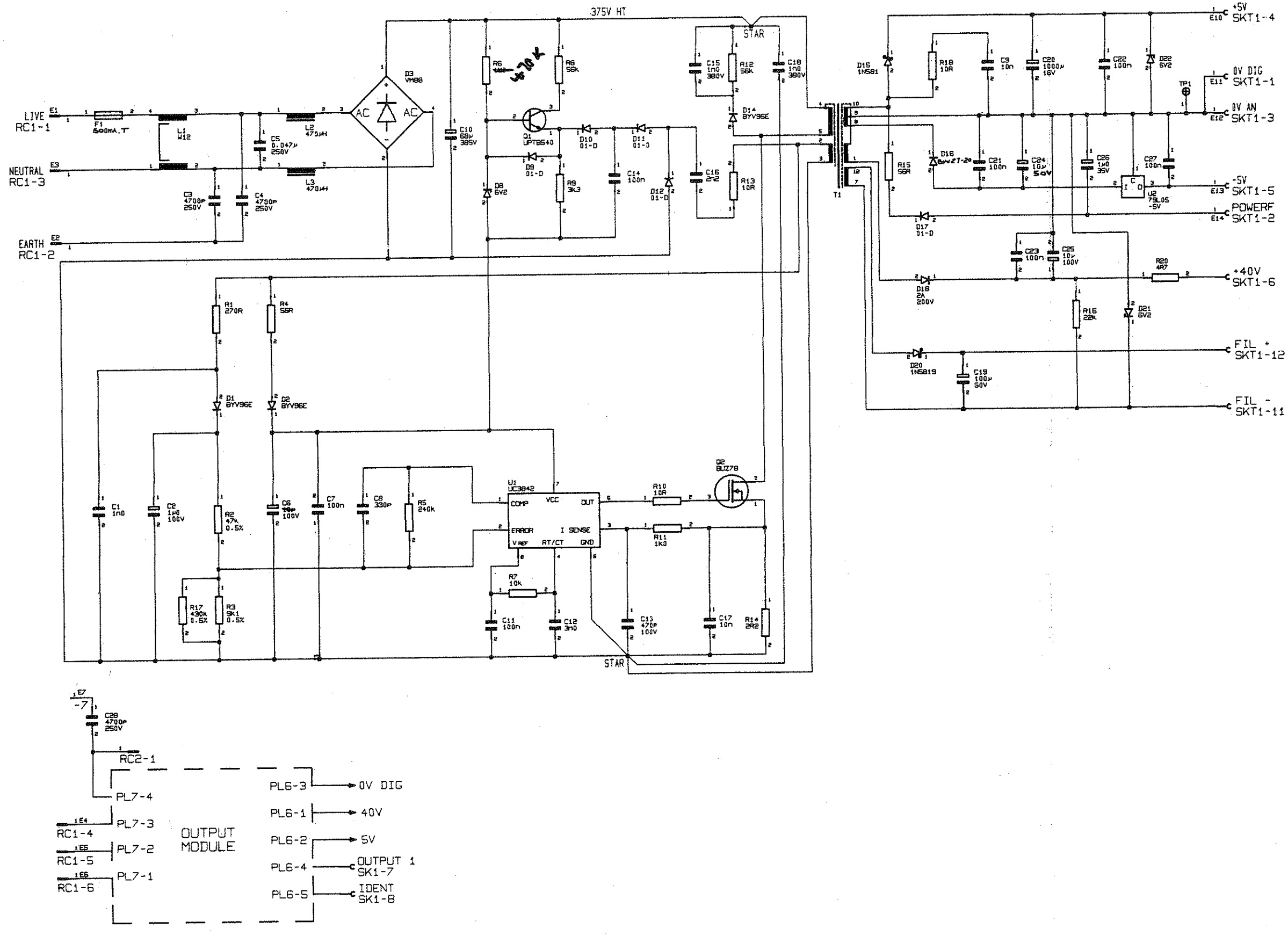


Figure 3 Power Supply Circuit Diagram
AI020979 Iss 4

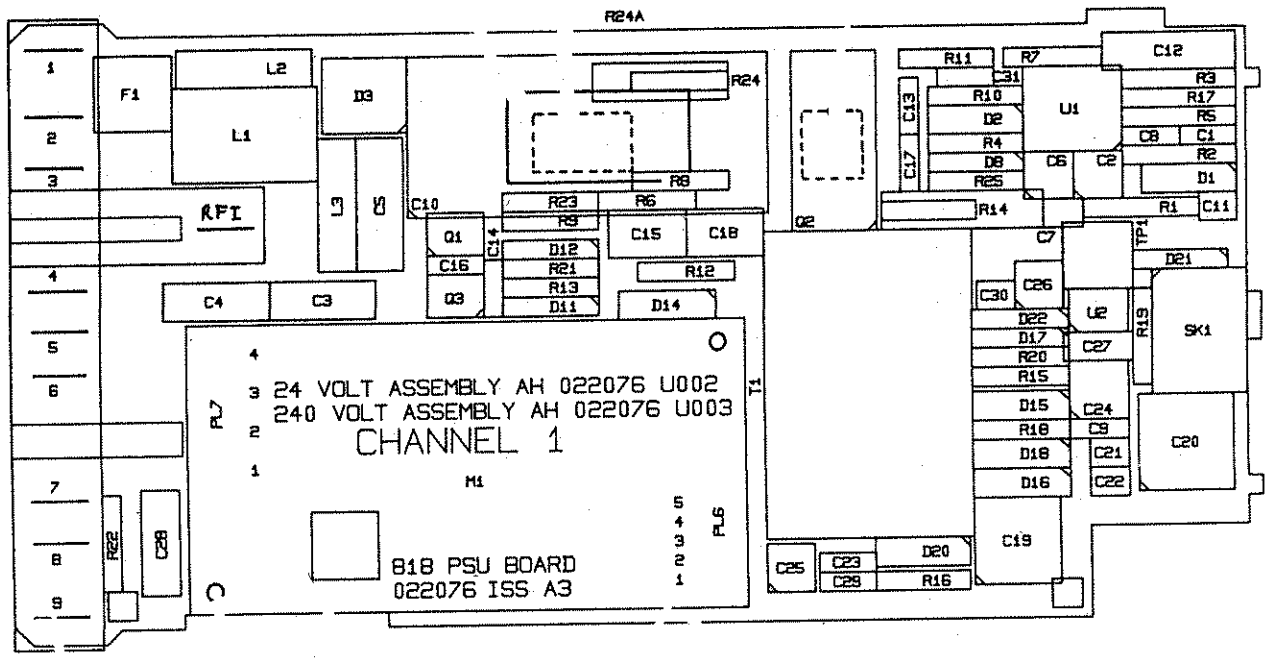


Figure 4. Power Supply 24V & 240V Layout - AH022076U001 Iss 4

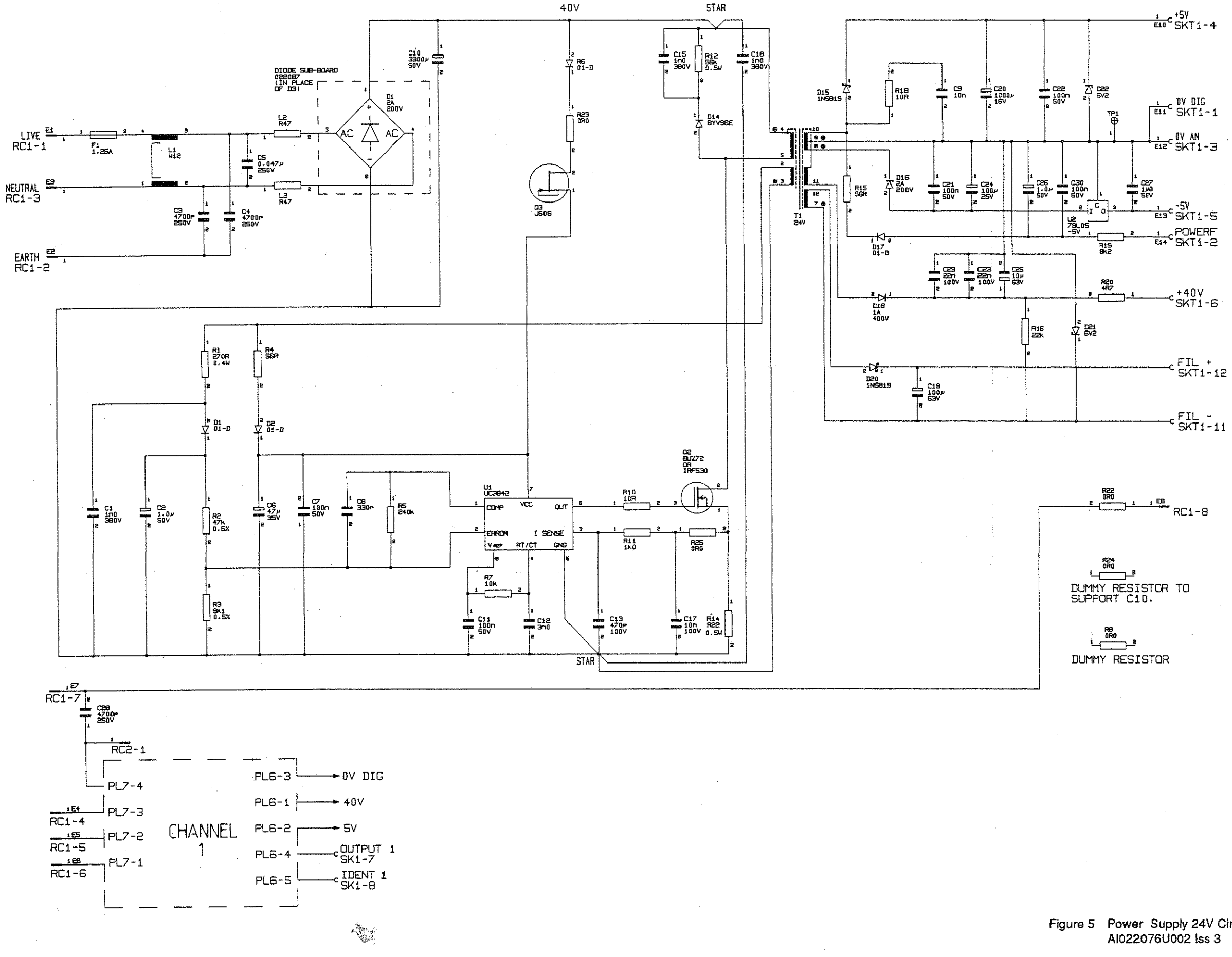


Figure 5 Power Supply 24V Circuit Diagram
AI022076U002 Iss 3

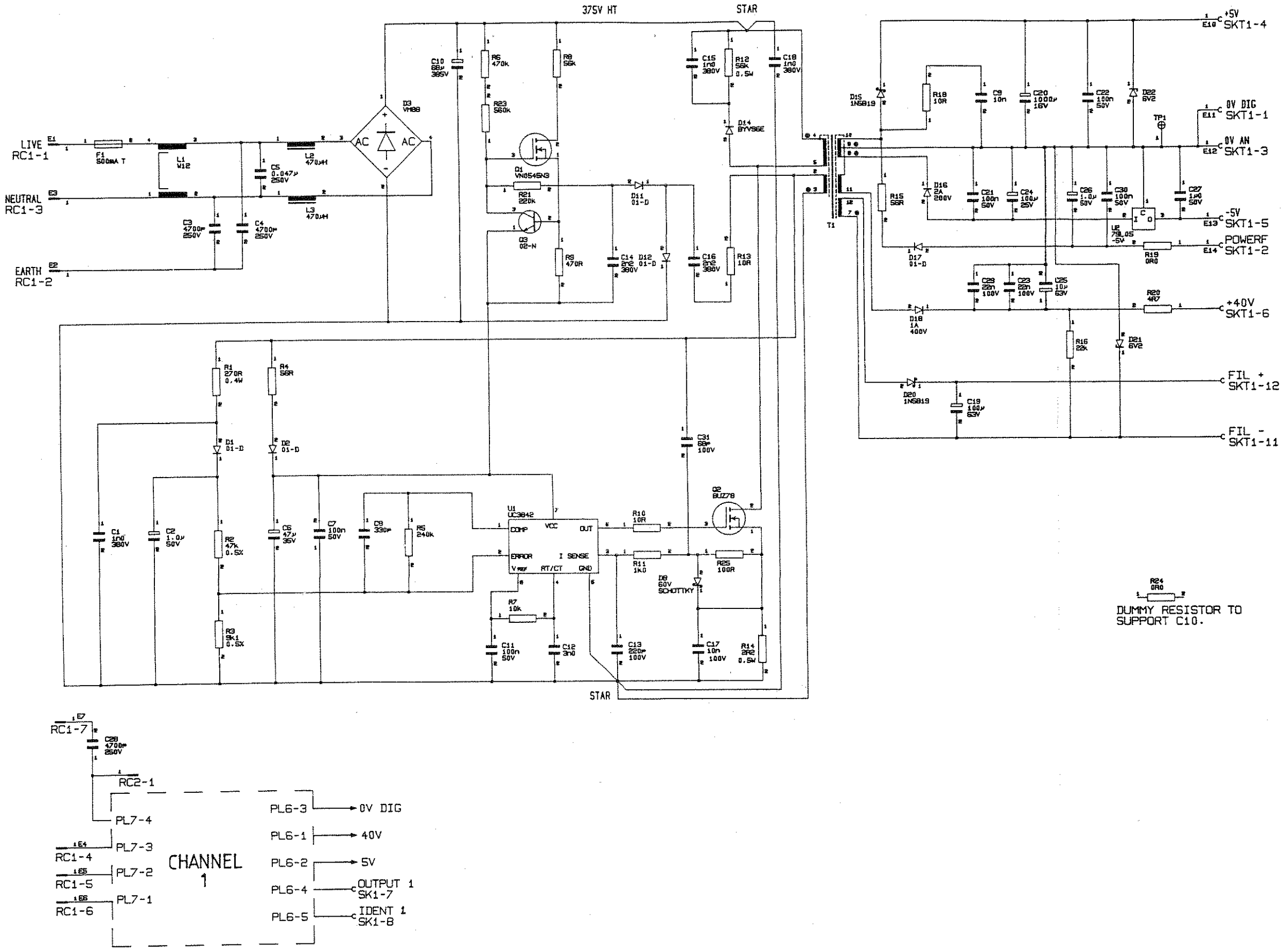


Figure 6 Power Supply 240V Circuit Diagram
AI022076U003 Iss 1

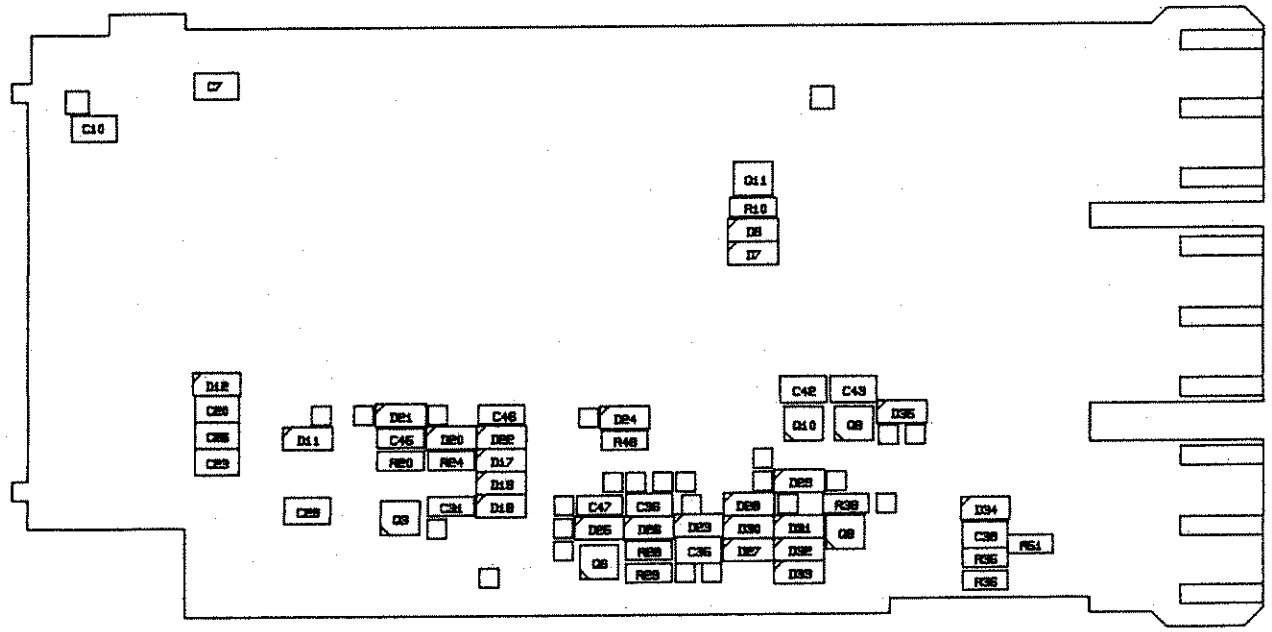


Figure 7. CNOMO Power Supply Layout (side 1) - AH021520, sht 1 Iss 1

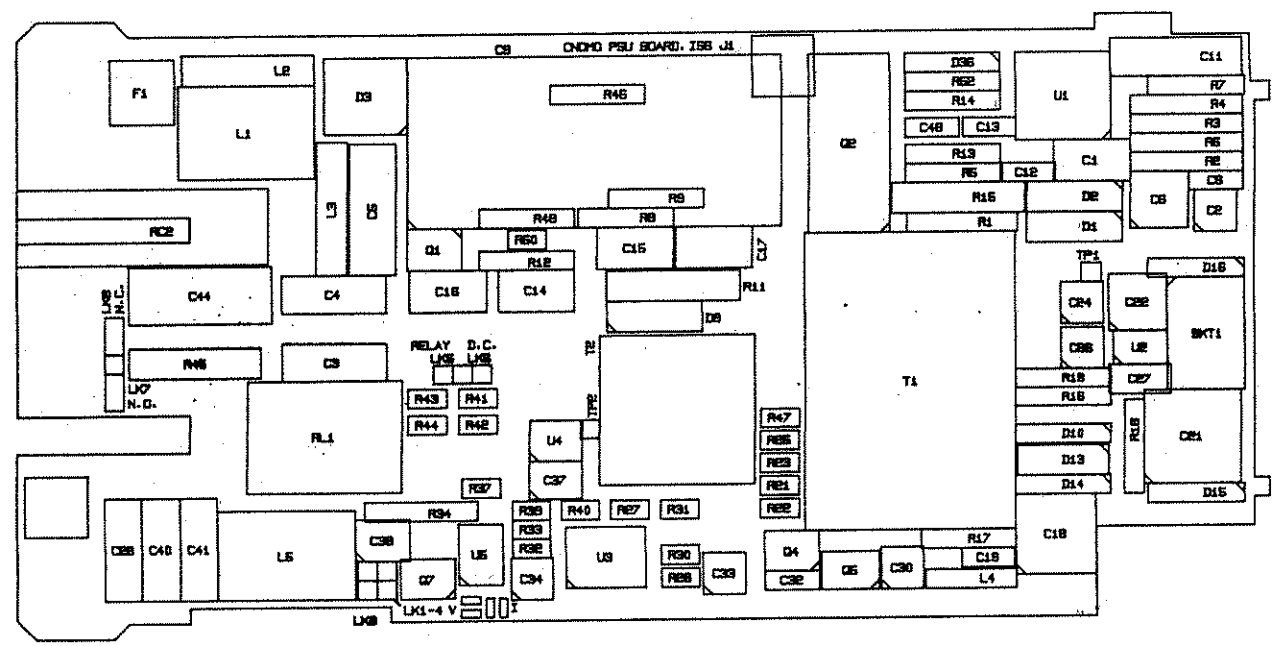


Figure 8. CNOMO Power Supply Layout (side 2) - AH021520, sht 2 Iss 1

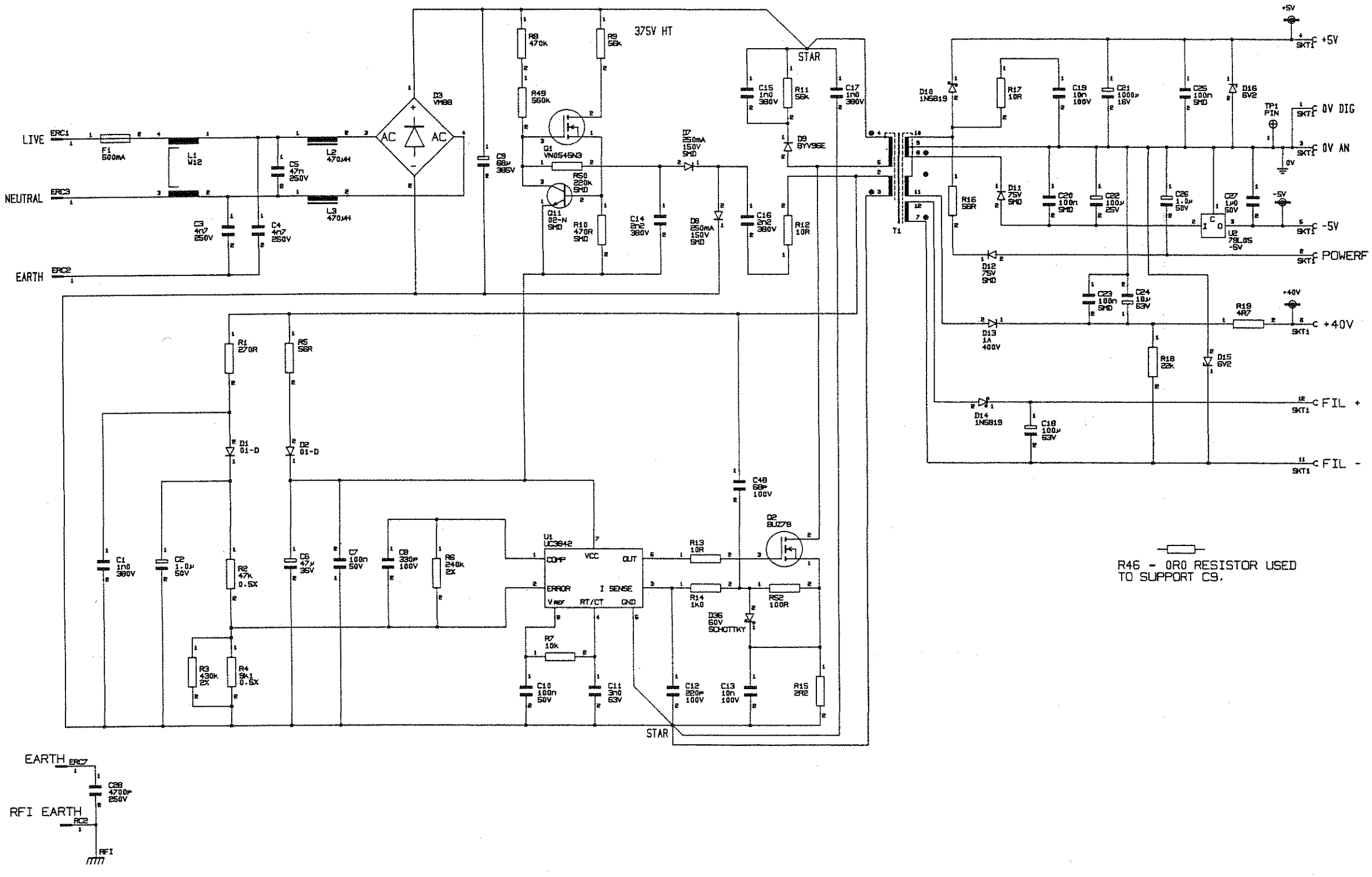


Figure 9 CNOMO Power Supply Circuit Diagram
AI021520U001 sht 1 Iss 1

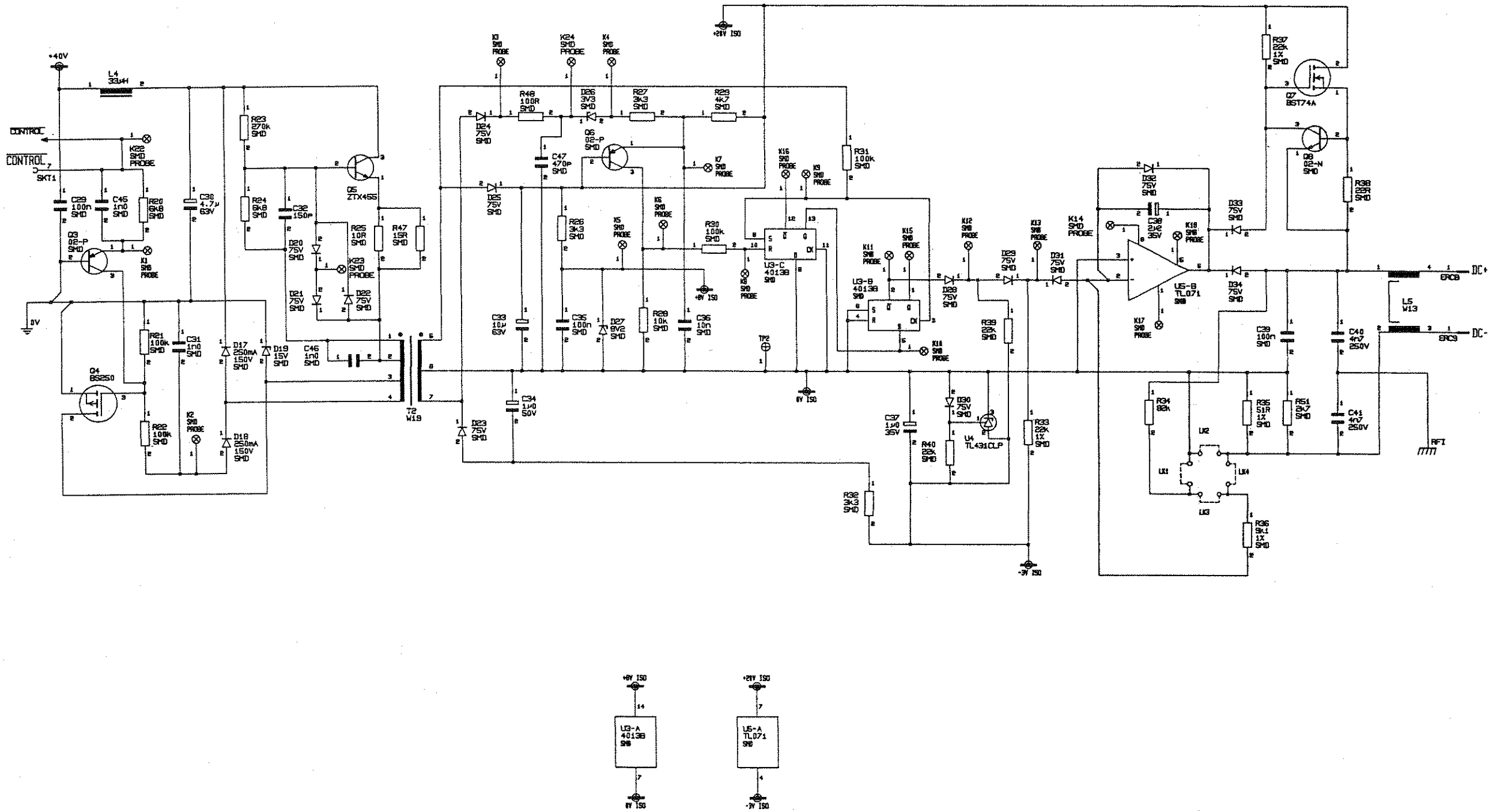


Figure 10 CNOMO Power Supply DC O/PCircuit Diagram
AI021520U001 sht 2 Iss 1

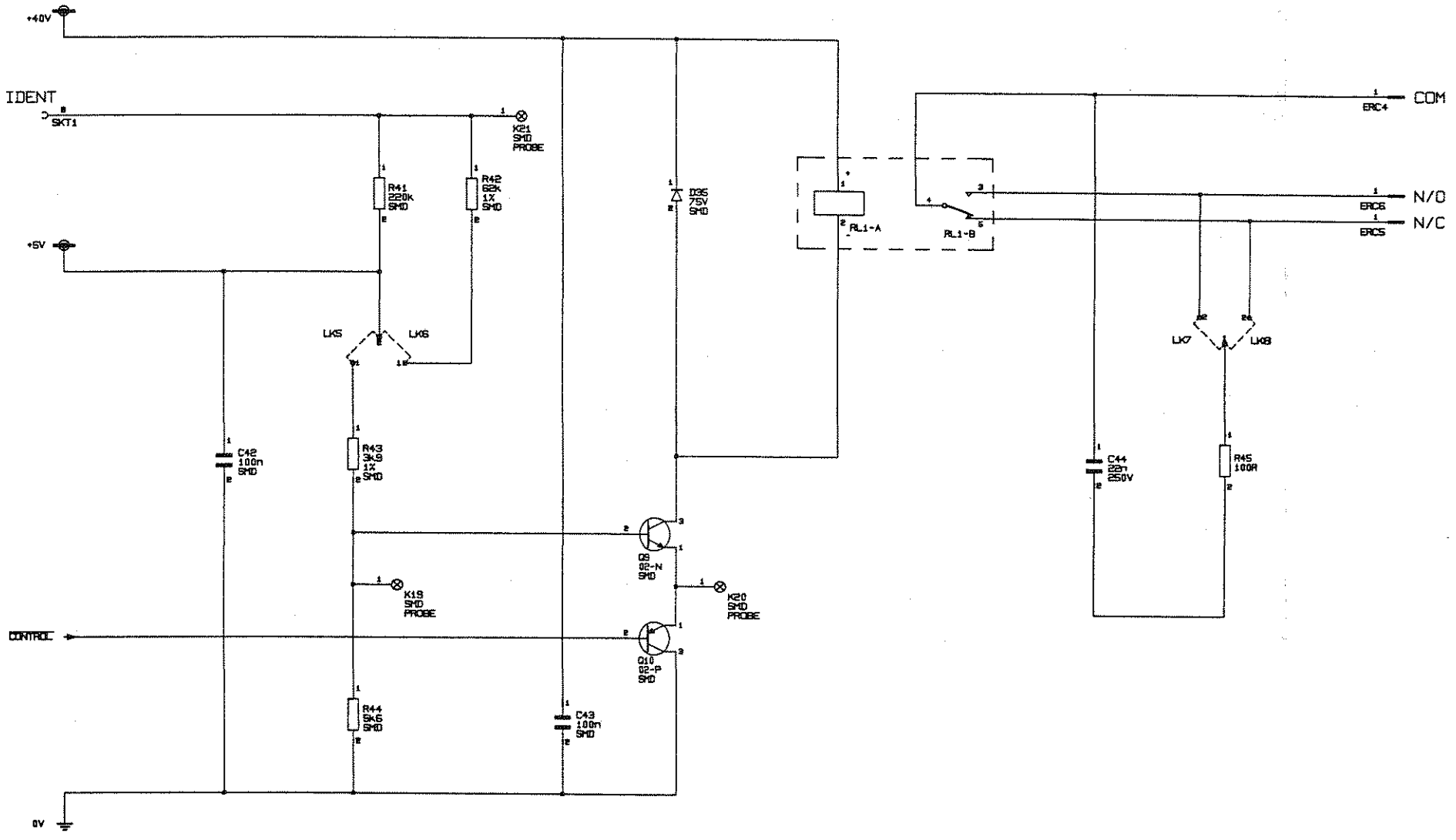


Figure 11 CNOMO Power Supply Relay Circuit Diagram
AI021520U001 sht 3 Iss 1

Chapter 4.0 **Microprocessor Board**

Contents

4.0 Microprocessor Board

4.1 Introduction

Two versions of the 815/818 microprocessor board exists. The original board fitted with the XICOR non-volatile memory (figure 3, 4, 5, 6 and 7) and the current board (figure 8, 9, 10 and 11) incorporating the DALLAS non-volatile memory.

The microprocessor printed circuit board is multilayered, and uses a mix of surface mount and conventional technologies to achieve the required component density.

The board layout is shown in figure 3, 8 and 10 with both sides of the board, conventional and surface mount components, shown. The circuit diagram has been split into two drawings figure 4, 5, 6 and 7 for XICOR and figure 9 and 11 for DALLAS. Figure 4, 6 and 9 shows the digital part of the circuit whilst figure 5 and 7 shows the analogue part.

Also included are two block diagrams figure 1 gives of the analogue part of the circuit while figure 2 shows the digital part of the circuit.

The first block diagram figure 1 shows the dual slop A/D convertor U15B with its comparitor U16B the analogue signal at low level being connected into the +ve input of U15B to obtain a high input impedance. U12B and U13B are two 8 way CMOS switches used to select the input to the A/D converter. The inputs to these switches are:-

1)	4 idents	- used to read the type of board in output 1 and 2 and alarm 1 and 2.
2)	3 +ve references	- used for the deintegrate part of A-D,which of 3 used depends on range.
3)	Power feedback	- to measure changes in supply voltage and identify low mains.
4)	3 -ve reference	- used to check stability of A-D converter. Which of 3 used depends on range.
5)	ZERO	- used to check on drift of A-D converter.
6)	CJC	- used to measure temperature of cold junction.
7)	Lead compensation	- used to make correction to RTD inputs for lead resistance.
8)	Input	- measures main process vaiable input.
9)	Remote	- measures a remote input after this has been isolated on the analogue communications board or dc Input board.

Also shown on the block diagram is a representation of the output voltage of the A/D converter U15B. The integrate period of each A/D converter is always 20ms. The time between the A-D conversions of the main process variable input is 125mS. Between each of these A/D conversions a measurement on one of the auxiliary inputs is carried out. These auxiliary inputs are measured in sequence regardless of whether the instrument has been configured for them.

The watchdog, reset and lockout sections of the microprocessor board are shown in figure 1. The power feedback voltage from the power supply unit is fed into U11-B and whilst the mains supply is above its absolute minimum value the watchdog is not activated by it. Port P3.5 out of the microprocessor is fed via a differentiator which charges C19 and holds the watchdog oscillator U14B off whilst activity is normal. If either of these inputs fails the watchdog oscillator will commence resetting the microprocessor. Ten milliseconds after the watchdog oscillator has been initiated U14C will turn the lockout line 'on' and disable the latch U3-B making its outputs go into the high impedance state which are then either pulled high or low depending on the position of links LK1, 2, 3 and 4. During power up the lockout signal disables the latch U3-B for a period of 3 seconds to allow the microprocssor to start up. During this time the display will indicate the version of software installed in the controller.

If the watchdog detects a software fault then the watchdog oscillator will operate for 10 cycles with an error message displayed. At this point the watchdog allows the microprocessor to try and recommence operation. If it is unsuccessful the watchdog will again give out 10 oscillations.

The board has 4 sets of links LK1 to 4 which set the state of output 1 and 2 and alarm 1 and 2 during start up and if the microprocessor fails.

There are also two switches on this board, one is for security enable and the other is for configuration enable.

Three other links, LK5, 6 and 7, are for future expansion and should not be fitted at this stage.
Two links, 8 and 9 are fitted on the Dallas board for memory expansion.

4.2 Features

1. Full software programmability for all configuration states
2. Links are available for unusual safe output states
3. No pots, all calibration being achieved in software
4. NVRAM and RAM technology for non volatile storage
5. Auto identification of the output modules

CONSISTS OF

1. 8032 CPU with 64k EPROM
2. 512 bytes non vol storage with protection circuitry on Xicor, and 2K or 8K on the Dallas.
3. 14 bit, 16 channel ADC with 9, 20, and 50 mV references
4. Reset, watchdog, and lockout circuitry
5. System I/O (including serial drive to the display)

The single processor controls all instrument functions including display and communications both analogue or digital.

The following key points with regard to the microprocessor PCB are intended for general reference purposes.

4.3 Digital Section

U1: Microprocessor
Port allocation as follows:

Ports 0 and 2 address and data (multiplexed)

Port 1
0. ADC input selection
1.
2.
3.
4.
5. Serial display drive - Clock
6. Serial display drive - Data
7. Serial display drive - Latch

Port 3
0. Serial comms receive line
1. Serial comms transmit line
2. Interrupt 0 - ADC end of conversion signal
3. Interrupt 1 - Power fail warning signal
4. NVRAM or RAM 'store' control line
5. Processor OK pulse line (watchdog)
6. Memory write control line
7. Memory read control line

U2: Address data demultiplex latch

The address LS byte is held at the output while the bus is used for data.

U3: Output latch

Resides at address 80xx, accessed by memory write to that address. Supports the following outputs

0. Comms transmit enable (RS 485)
1. Sensor break current enable
2. NV write protect line
3. Channel 1 output (normally OP1)
4. Channel 2 output (normally OP2)
5. Channel 3 output (normally AL1)
6. Channel 4 output (normally AL2)
7. Retransmission output

Miscellaneous Gating
U9d and U10d with reset and A15 disables U4b (memory decoding) until reset is inactive and A15 is high.

U10b and U10c prevent a read from NVRAM while its control line NE is low. This prevents an inadvertant recall of non vol data into its RAM area.

U9b allows a write to the output latch only when addressed and a write operation is being performed by the µP.

U9c and U10e prevent a write to non volatile memory unless enabled by a low at Q2 of U3 (non volatile memory write enable) and a µP write operation.

Writing to config area address 8600 to 867F. Writes are normally inhibited to this area by U4 and U10. The closure of the config switch disables U4 thus enabling write access to this area.

Miscellaneous Details

Xtal frequency is 11.0592 MHz for comms baud rate generation.

Open inputs to the PCB are often tied up for increased protection from static during handling.

Links 1 to 4 determine the state of the outputs when instrument powers up or enters the lockout mode. The default for these links is position 'a' (ie inactive). For an active output when in either mode, fit link in position 'b'. Note that outputs are active low.

4.4 Analogue Section

U11: Voltage comparator for power fail detection

The comparator U11 and circuitry compares the power feedback voltage with the a reference. When the mains voltage drops to below approx 75V the output goes low generating a power fail signal.

U14: Reset watchdog and lockout

The output from U14b (reset) is high while U11 output is low. When U11 output goes high (signifying the presence of sufficient mains voltage) the output of U14 goes low de-activating reset allowing the processor to function. Normally a pulse is issued from the processor to indicate that all is well and this pulse forces C19 to charge, holding the output of U14b high. In the event of the pulse not appearing, the circuit configuration around U14b allows the output to oscillate thereby resetting the processor and allowing it to run until a pulse is issued holding it out of reset. When U11 output goes low, the pulses from the µP holding C19 high are inhibited and C19 discharges through R37. There is therefore a delay between the power fail signal from U11 and the reset (U14b output going high when C19 is discharged). During this time the µP finishes any current activity and stores the contents of NVRAM in the non vol area.

The lockout action is performed by U14c and associated circuitry. This circuit monitors the microprocessor reset line, and if too much activity occurs then the output of U14c goes high allowing the instrument lockout to become active. Lockout is active when C20 is discharged. This occurs under the following conditions:

1. Power up
2. Extended reset oscillation (µP failure)
3. Instrument error flash mode (causes reset to oscillate)

C15: Additional hold up time for the reset circuit supply is provided by C15.

U15:
U16: A to D convertor section.

4.5 Analogue to Digital Converter (ADC)

The ADC is dual slope. The integrator is formed by U15 and C21 with R68 and R71 forming the resistance. Reset is performed by the FET Q4. End of conversion is detected by U16b and fed to the microprocessor interrupt pin via Q5. The configuration of the circuit is a non inverting integrator giving a high input impedance. Unfortunately the input signal also appears as an offset in the output. This is cancelled by routing the input signal also to the comparator so only the integral term is being monitored by the comparator. The input signal is routed to the integrator with no pre-amplification making this a low level converter.
References and positive supplies are generated by the circuitry around U16c. D12 is a bandgap reference of 1.26V which supplies reference circuitry around the instrument and particularly the ADC reference. This reference is inverted and presented at the output of U16c via Q7 and D11, within the feedback loop giving an overall gain of 2. This supplies a clean stable supply for the integrator and for the deintegrate voltage.

U12:
U13: A to D convertor input multiplex switching

The input switching necessary to the ADC is provided by U12 and U13. Inputs are as follows:

U13

Measured value
RT lead comp measurement
Remote analogue input
ADC zero measurement
ADC reference 8, 20, 50mV

U12

ADC deintegrate voltages for the 3 ranges
Power feedback signal
Hardware ident signals (4 lines)

ADC - Conversion Details

Two conversions are performed every 125ms, the first of which is always a measured value conversion.

The second conversion is an auxilliary conversion, being one of the following:

Zero
Reference (for configured range)
CJC or lead comp (as configured, default to CJC)
Power feedback
Remote input
Auxilliary (pot position) input

Each of these conversions is performed in turn, always, irrespective of instrument configuration.

The deintegrate voltage used is that for the configured range which is the same for all conversions.

The pot position input comes down the ident line of channel 4.

Idents are only exercised during power up, during which time the value of the ident voltages coming from the fitted modules is measured. For this reason they are not considered (with the exception of pot position) in the above.

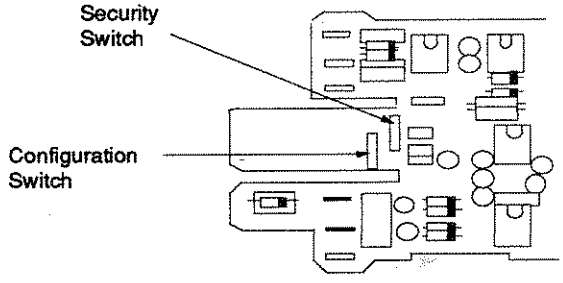
Miscellaneous Details

Thermocouple break current is supplied when Q6 is turned ON by the microprocessor. Note that this allows the removal of this current when not required, ie for non TC inputs and during calibration. (The offset due to this current and mV source internal resistance could otherwise cause errors).

CJC is performed by the 1N4150 diode D13.

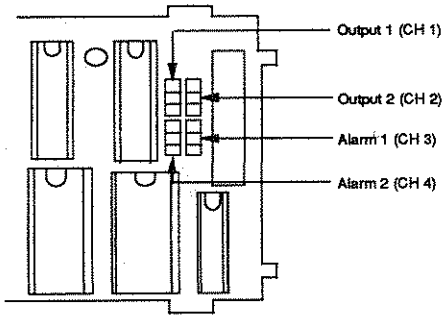
4.6 Switches and Links

The microprocessor board contains two ON/OFF switches, one for configuration selection and one for display security.



Instrument Configuration and
Security Switches

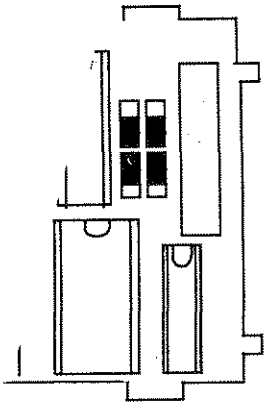
Four sets of change-over links are fitted to this board. Each set of links is assigned to one of the four outputs as shown above. These links set the condition of these outputs during the 'power up' period and also during a reset of the main microprocessor.



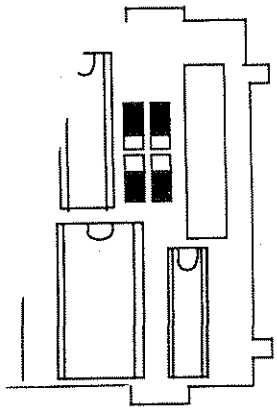
Links defining the output and Alarm
condition whilst in reset

The position of the links for the two output states is shown below.

Position of links for :
Outputs or retransmission giving zero output from rear terminals.
Alarms going to the de-energised condition.

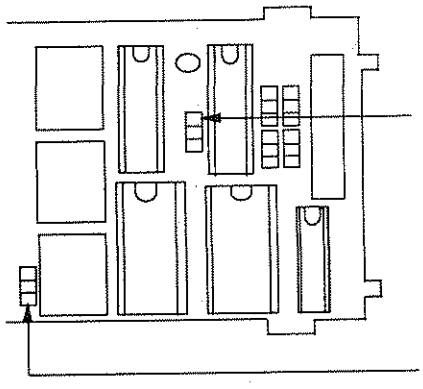


Position of links for:-
Outputs or Retransmission giving maximum output from rear terminals
Alarms going to the energised condition

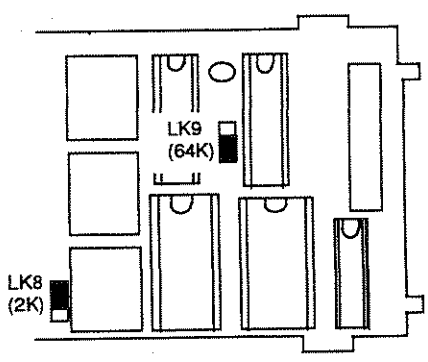


Default
This is the way that all these links are set when the instument is delivered from the factory.

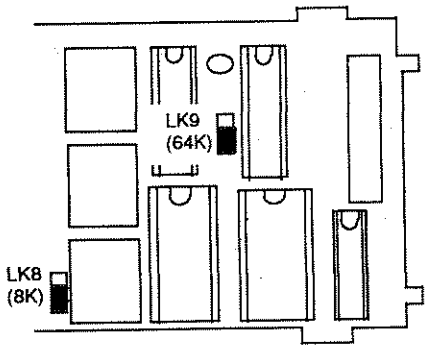
Position of links for setting memory sizes on Dallas type board.



Default
This is the way the links are set when the instrument is delivered from the factory.



2K



8K

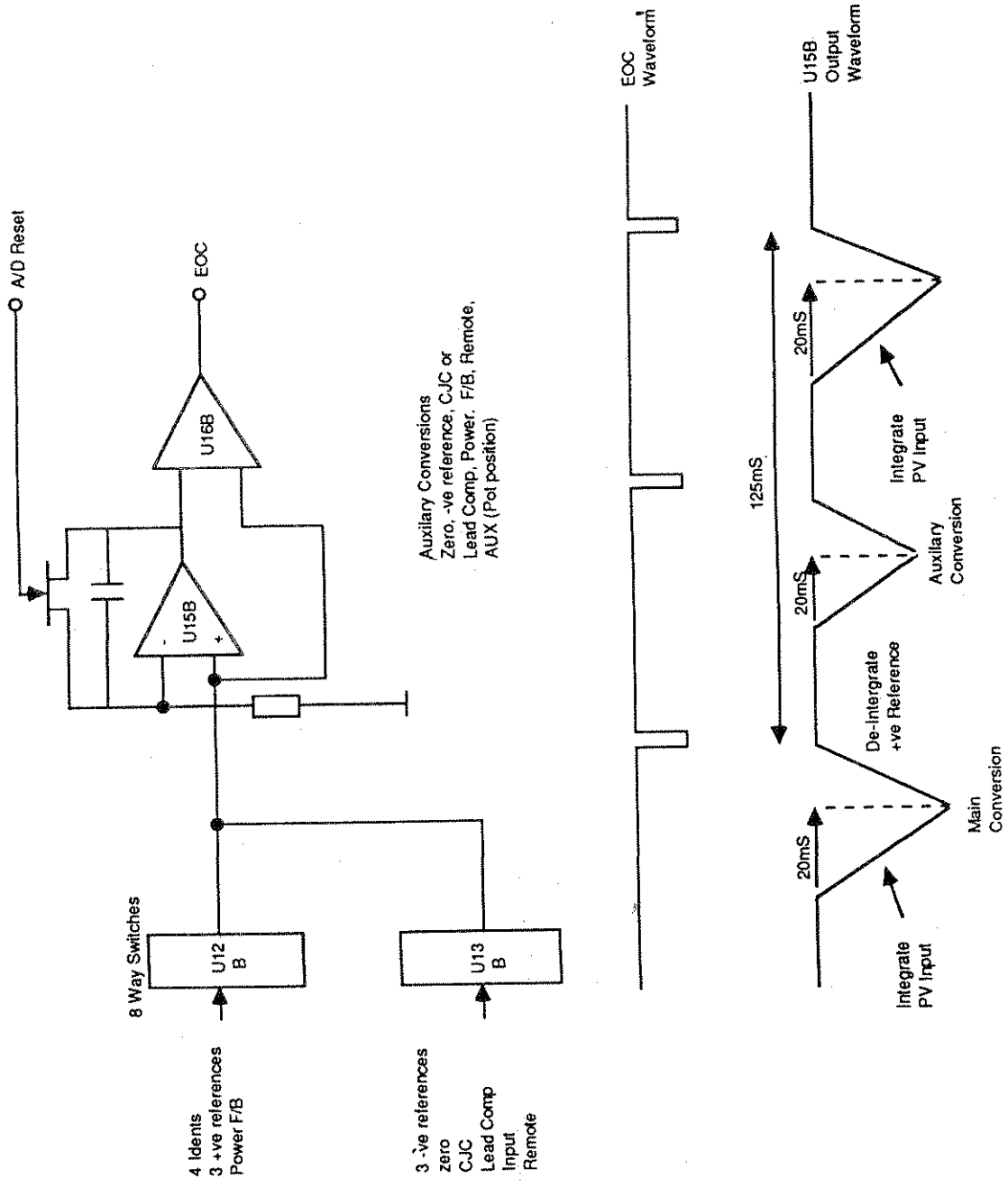


Figure 1. Microprocessor Block Diagram (Analogue Section)

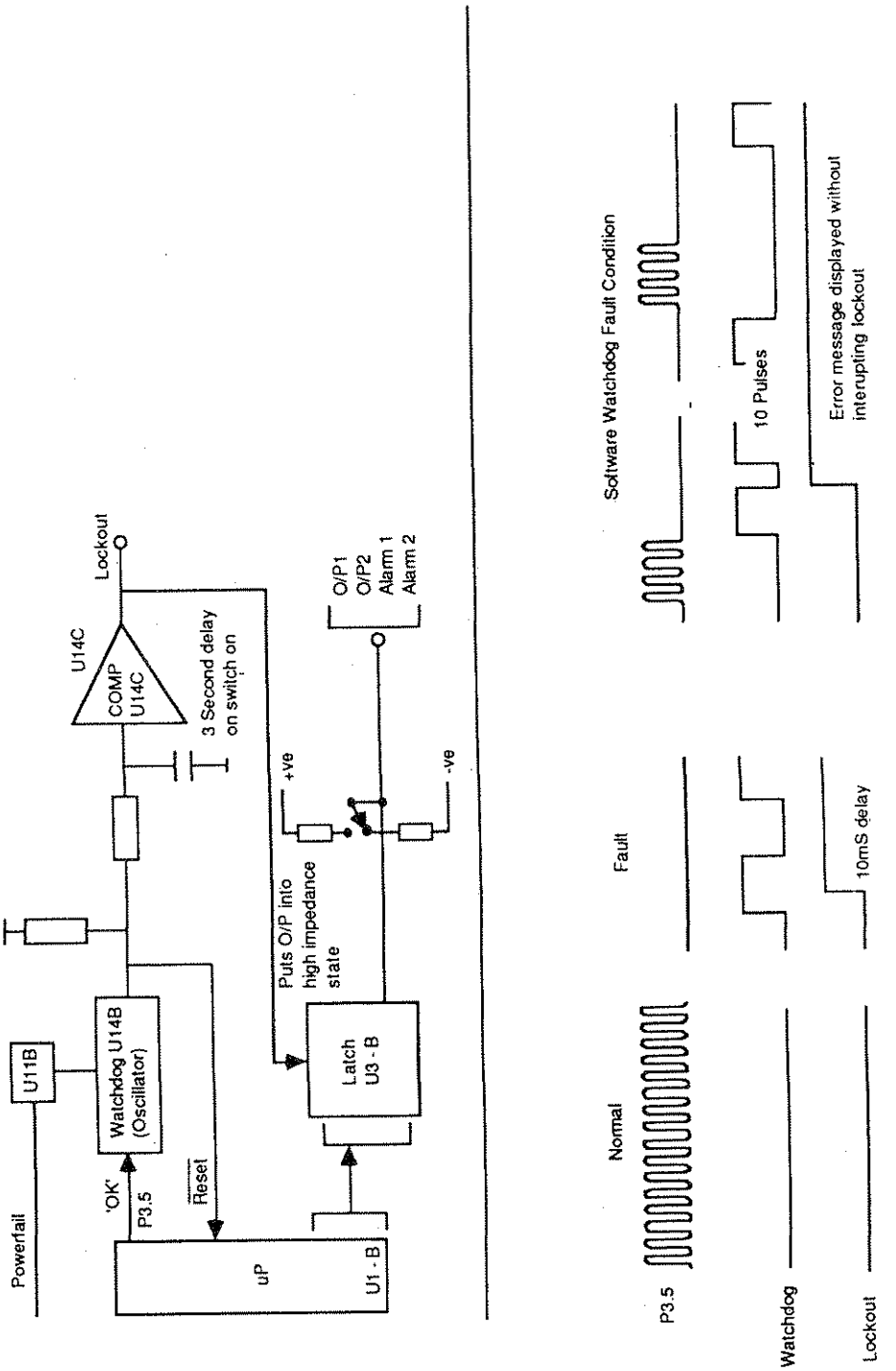
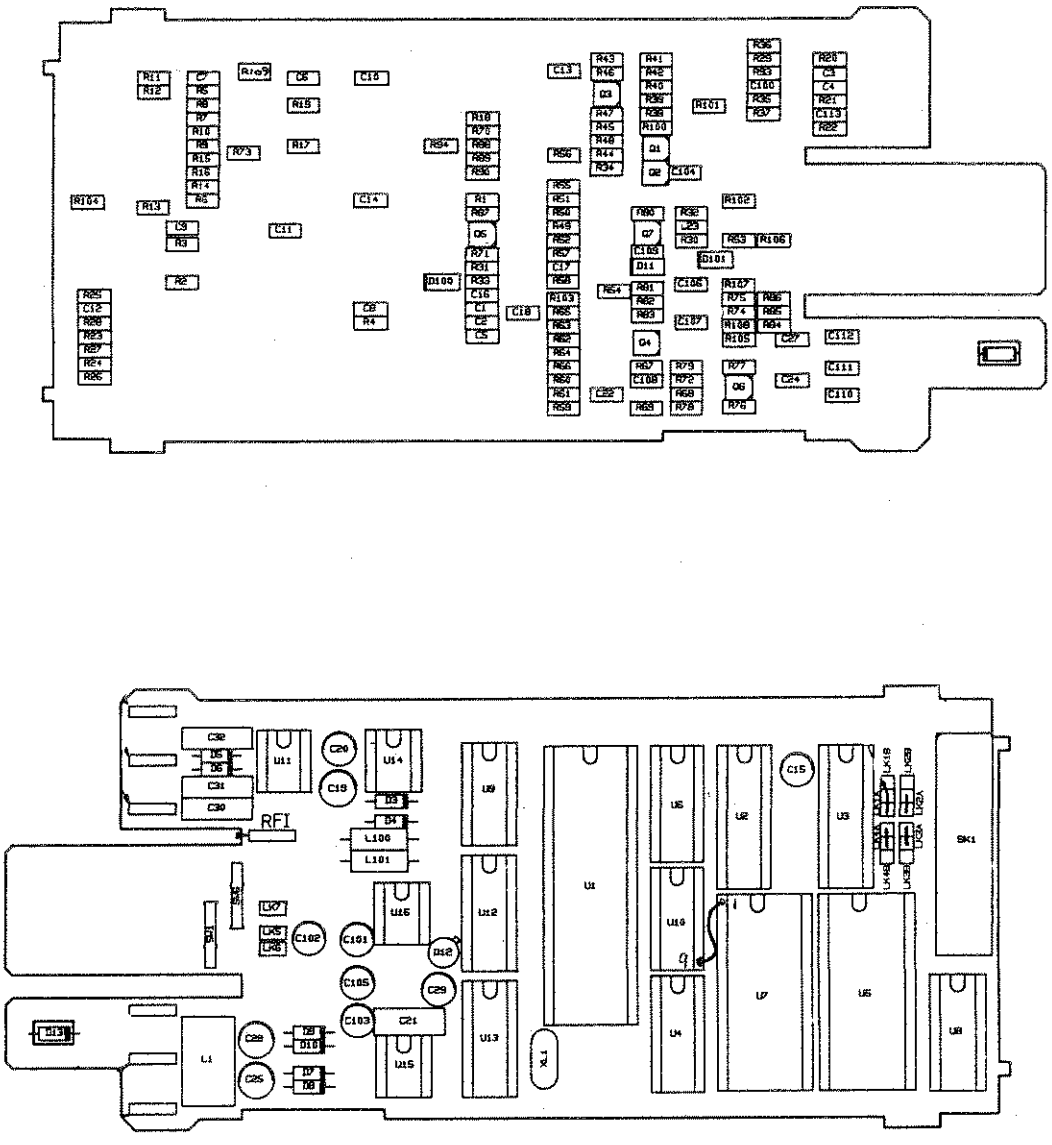
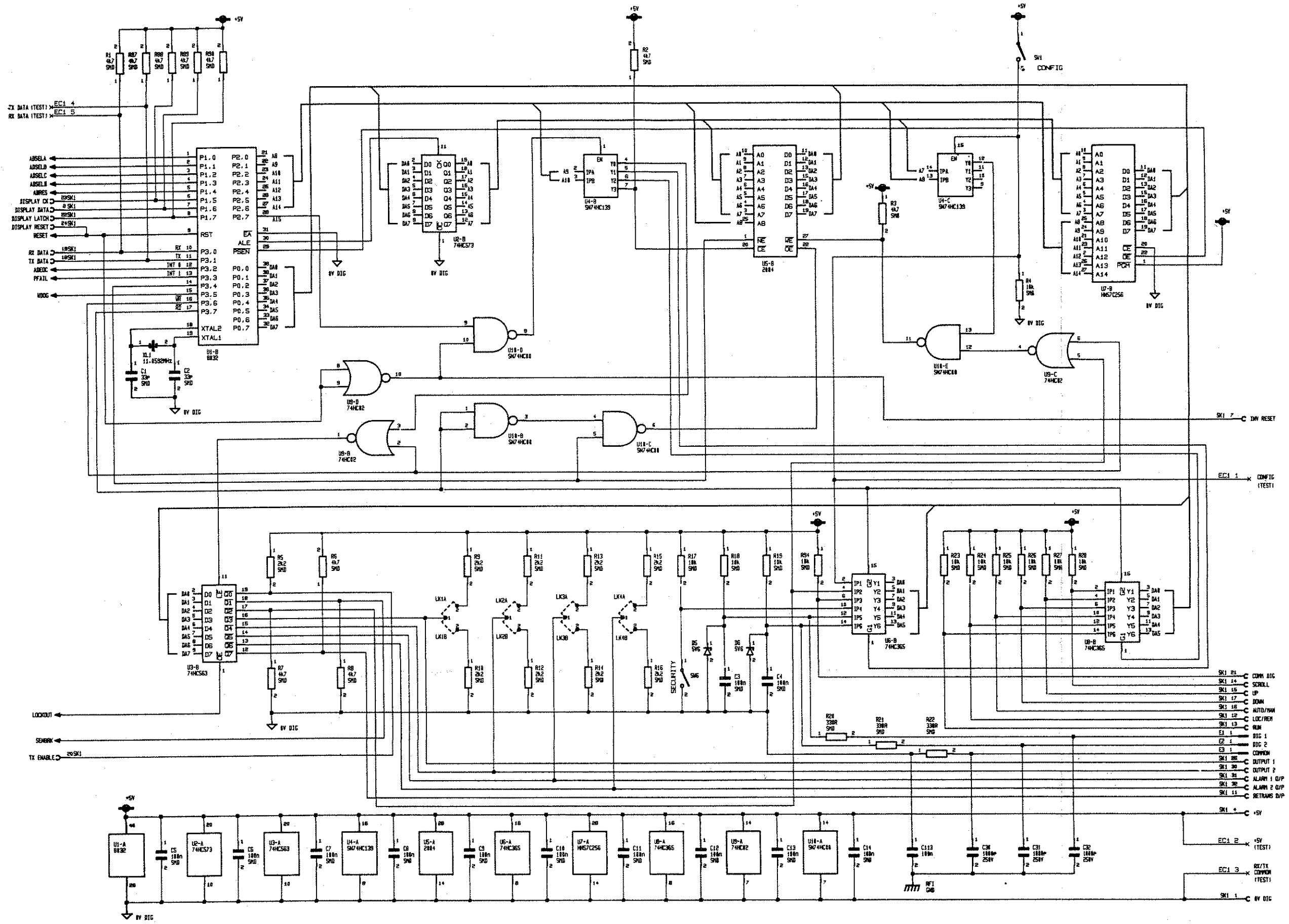


Figure 2. Microprocessor Block Diagram (Digital Section)



Note 1: Pin 1 of U7 is connected by a flying lead to pin 9 of U10 when a 64K ROM (27C512) is fitted.
Note 2: R105, R107 and R108 resistors are not fitted to current 1989 versions.

Figure 3. Microprocessor (Xicor) Board Layout AH020989 Iss 3



* Pin 1 of U7 is connected by flying lead to pin 9 of U10 when using 64K ROM. +5V is still present at pin 1 of U7 socket.

Figure 4 Microprocessor (Xicor) Circuit Diagram
AI020989 sht 1 Iss 5

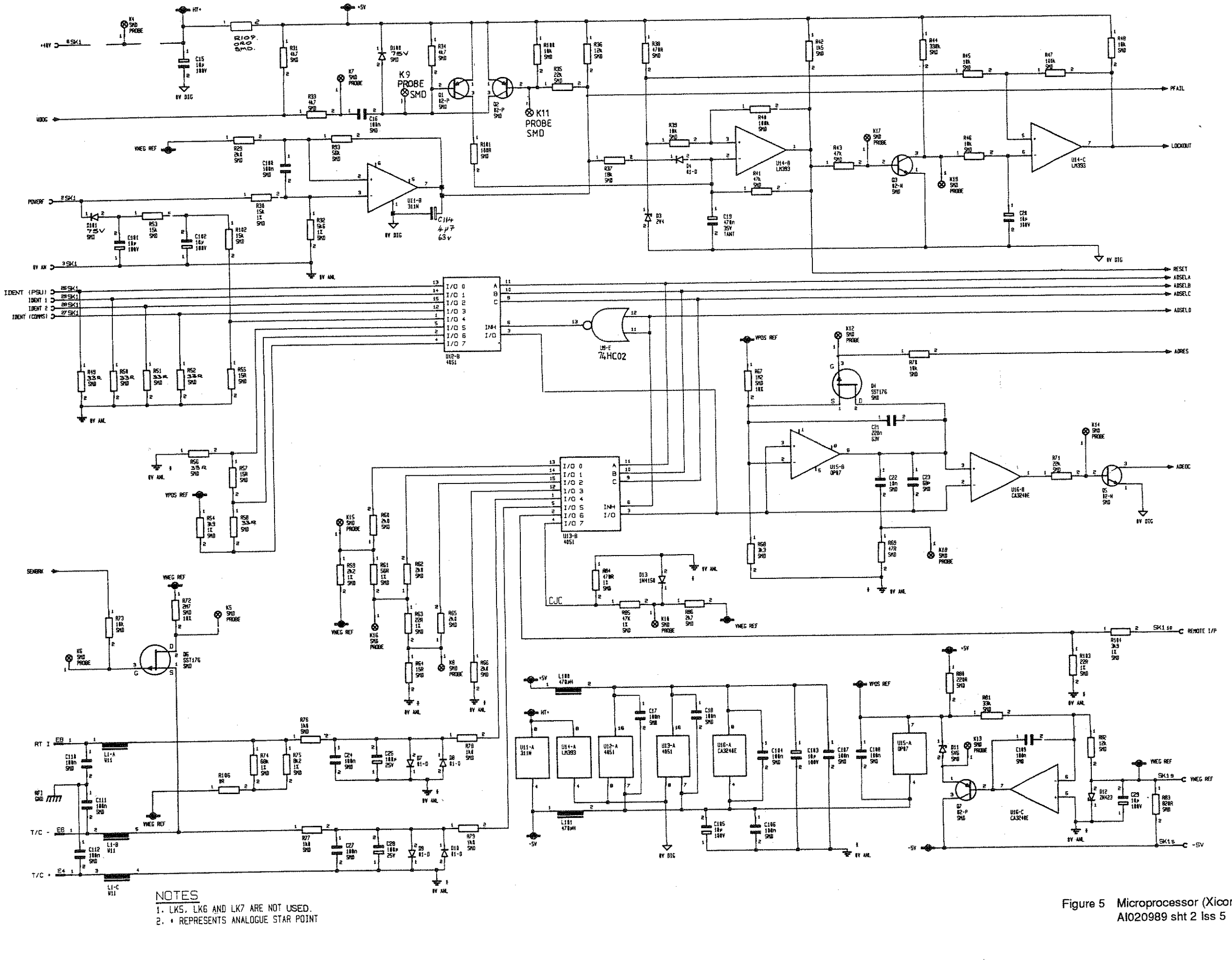


Figure 5 Microprocessor (Xicor) Circuit Diagram
AI020989 sht 2 Iss 5

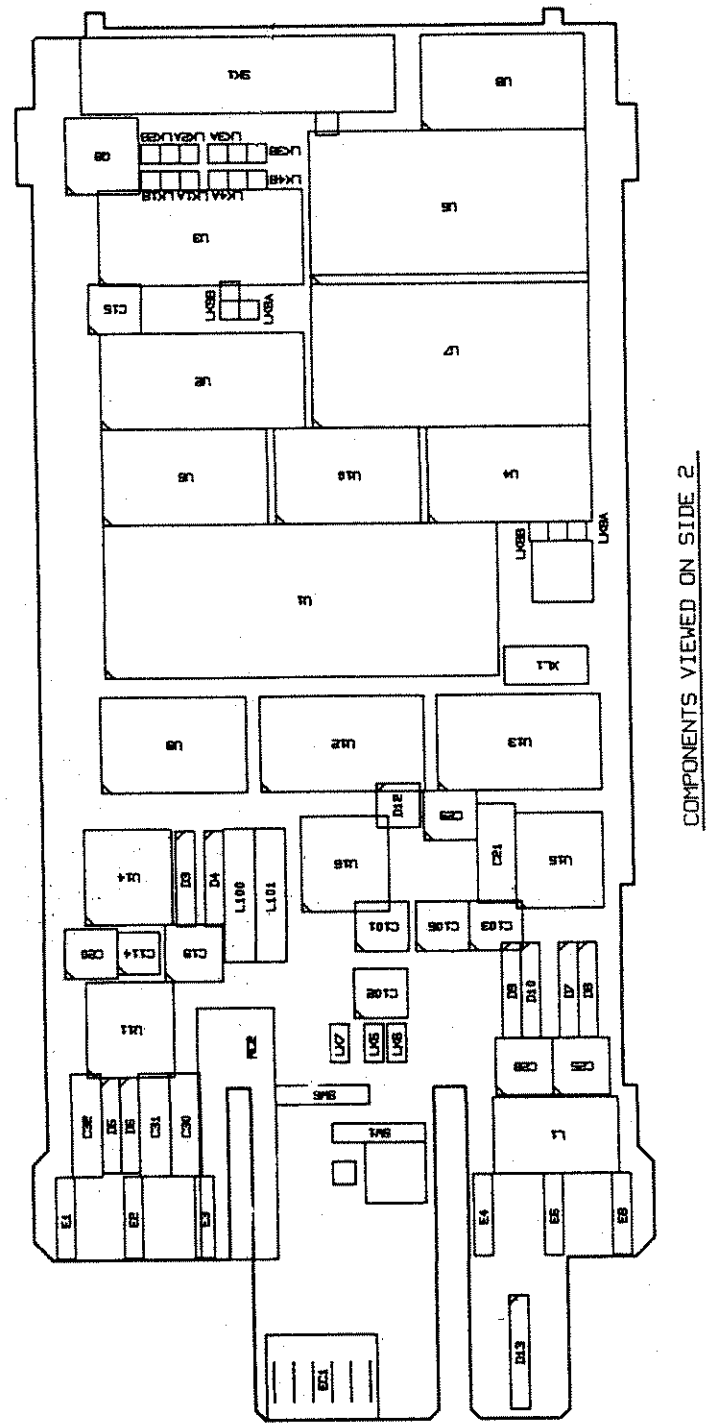


Figure 6. Microprocessor (Dallas) Layout AH022073U001 sht 1 Iss 4

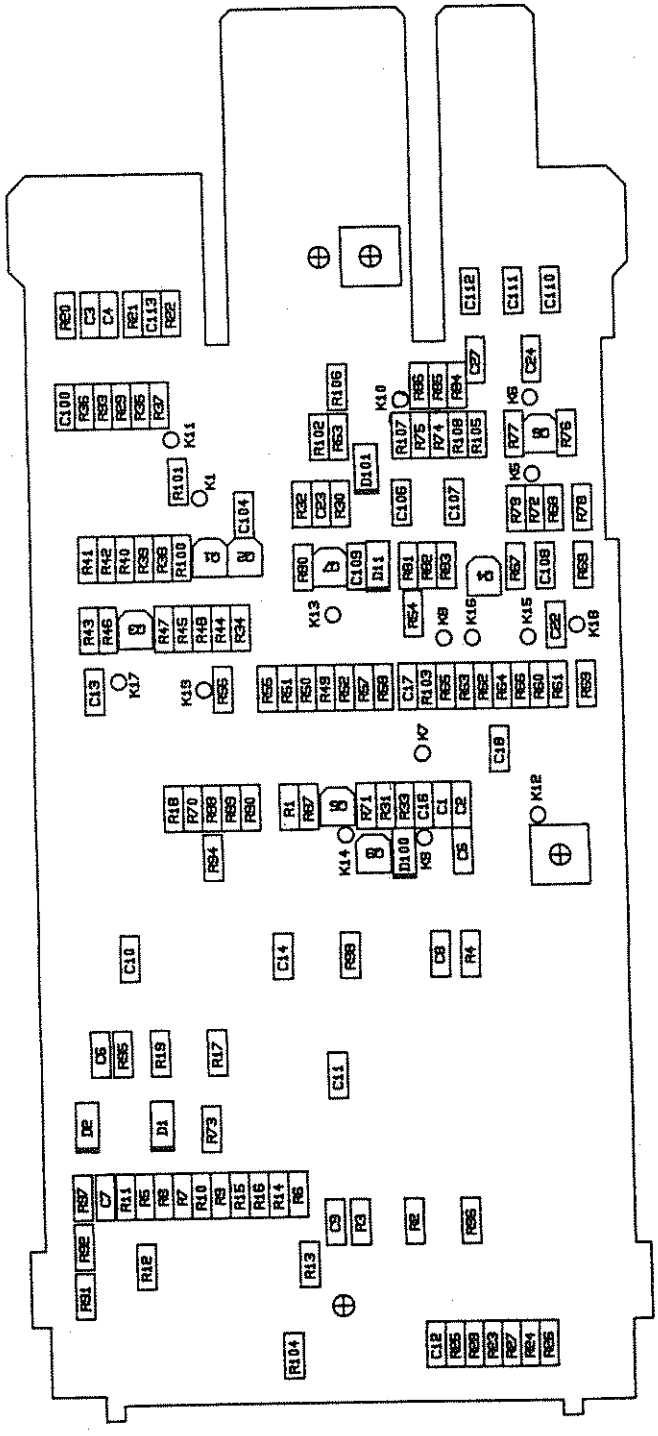


Figure 7. Microprocessor (Dallas) Layout AI022073U001 sht 2 Iss 4

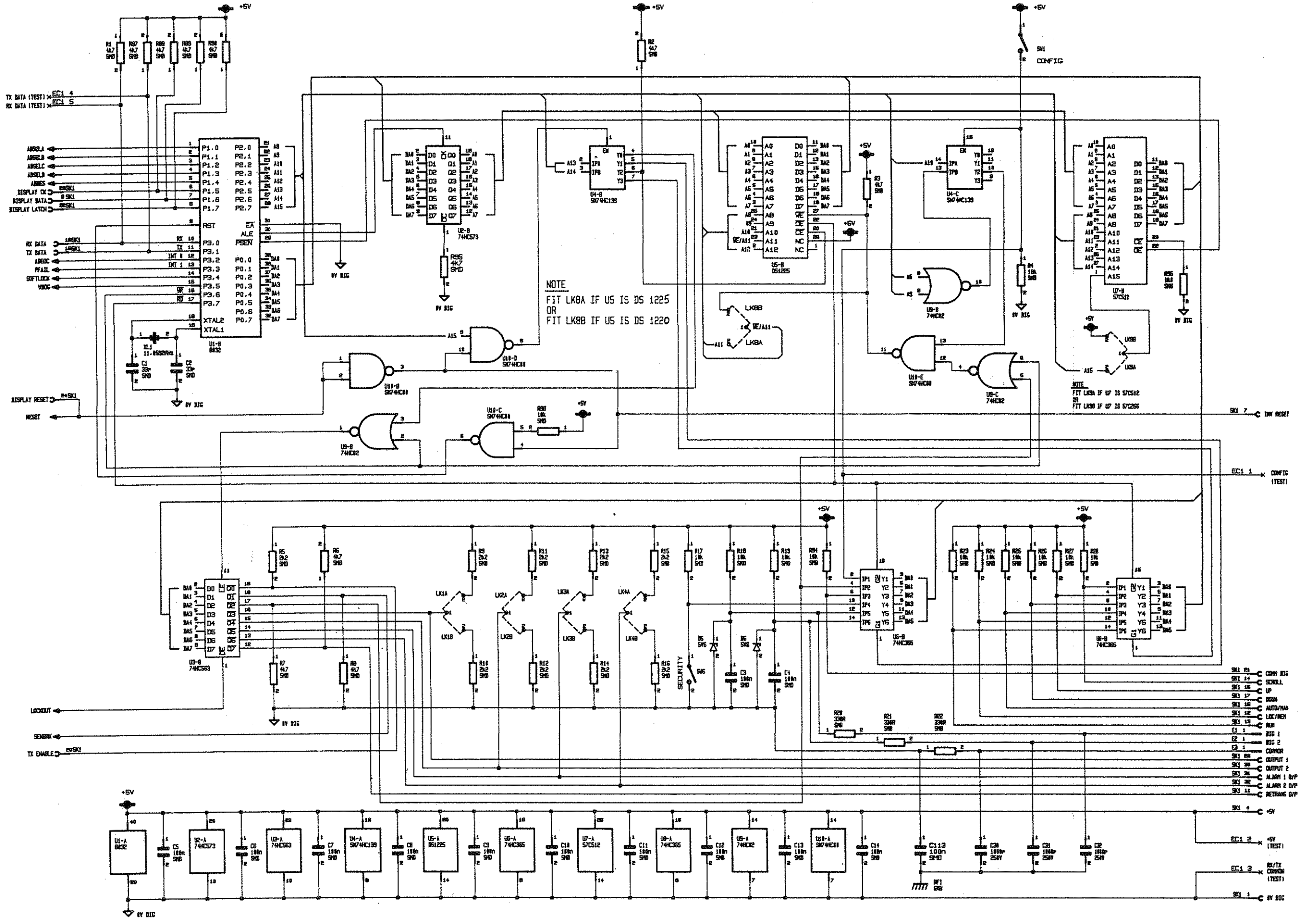


Figure 8. Microprocessor (Dallas) Circuit Diagram
AI022073U001 sht 1 Iss 4

Chapter 5.0 **Communication Boards**

Contents

5.0 Communications Boards

5.1 Digital Communications Board

5.1.1 Specifications

Operating temperature range:

0 - 70°C

Power Supplies:

40V + 15%, - 5%
5V +/- 10%

Input Signals:

DIG IN 3. A digital input with volt free contact closure operation -
LOGIC IN 3 is 1V when the contact is closed with 100R impedance or 1V is applied.
LOGIC IN 3 is 3V when the contact impedance is 20K or 3V is applied.

RX is a standard RS232 or RS422/RS485 input.
RX DATA is the corresponding non inverted TTL output (0<Low<1V; 3<High<5.5V).

Output Signal:

TX is a standard RS232 or RS422/RS485 output.
X DATA is the corresponding non inverted TTL input (0 <LOW< 1, 3 <HIGH< 5.5V).

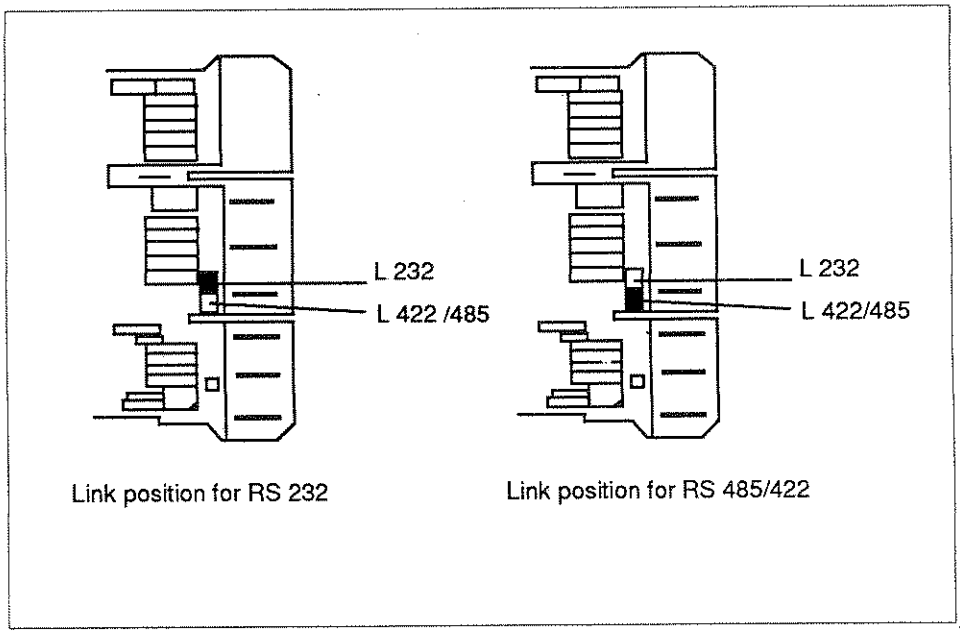
NOTE: DIG IN 3, RX and TX are isolated from the instrument to 264V and meets IEC 348 but not from each other.

Hardware Links

One to change

RS232 - RS422

The digital communications board contains a changeover jumper, for the selection of RS232 or RS485/422 type.



Link position for RS 232

Link position for RS 485/422

5.1.2 Introduction

The layout of the digital communications board is shown in figure 9 whilst the circuit diagram is shown in figure 10.

A block diagram of this digital communication board is given in figure 1.

The information for the digital communications link is handled by the microprocessor. The correct drive, current limit and isolation of these signals are accomplished on the digital communication board.

The powering of the isolated portion of the circuitry is derived from a 100KHz oscillator. This frequency is divided by two before it is used to drive the isolator transformer. The secondary of the transformer is rectified to power the isolated circuitry. The frequency of the oscillator can be doubled, this being detected by a discriminator on the secondary of the transformer and used to disable the transmission of data.

A digital input brought into the rear terminals of the instrument is also taken via an opto-isolator to give isolation from the rest of the controller. This input is also read into the micro-processor and is also used to disable the front panel lockout.

One link is mounted onto this board and that is used to convert the communication standard from RS232 to RS422 (485). The link positions are clearly marked on the board.

5.1.3 Features

This board has both RS232 and RS422 transmit and receive facilities. Selection of transmit mode is done by a hardware link. The receive circuit is compatible with either. Interface to the microboard is by three signals: transmit data, receive data, enable. The latter controls the transmit/high impedance state of RS422 transmit. The circuit is electrically isolated from the rest of the instrument. A transformer is used to transfer power and RS422 ENABLE across the isolation barrier, and two opto-isolators are used for transmit and receive data.

5.1.4 Power transfer and encoding of RS422 ENABLE:

TX1 primary is push-pull driven from the 40 volt supply by two VMOS devices Q1, Q2; the frequency of operation can be switched between two values of ratio 2:1. The frequency conveys RS422 ENABLE. The initial oscillator is a 555 timer 1C, U1, and associated components. The frequency of oscillation is approximately 200 KHz. U2 is a dual J-K flip-flop whose two sections in cascade divide the 555 output frequency by 4. If, however, J,K inputs of the second stage are held high, it will toggle at every +ve edge from U1. The result is a divide by 2 instead of 4, ie double the frequency. This is indeed the default mode since R4 pulls up SET input of U2-B setting Q output high. With RS422 ENABLE active low, the first J-K flip-flop is free to toggle with U1 clock +ve edges, and W1, W2 are driven at 1/2 the default frequency from U2-C complementary outputs. To secure against a period of simultaneous conduction characterised by excessive simultaneous device current U2-C +ve edges (U1 or Q2 turn-on) are delayed by R7 or R8 acting with the self-capacitance of each gate. The -ve edges (causing output device turn-off) are not delayed, but are passed to their respective gates by diodes D1 or D2.

L1, C3, C4 are a pi-filter to minimise current spikes being inflicted on the 40 volt line which might otherwise upset low-level processing parts of the instrument.

The three isolated supplies +14V, -14V, +7V are generated by rectifying and smoothing TX1 secondary (D3-D8, C5, C6, C8).

Receive Data:

U6-C and associated components are the data receive circuit for either RS232 or RS422. With RX+, RX- left disconnected, R38-R41 values are such that U6-C inverting input is more +ve than the non-inverting input, and therefore the comparator output (open collector) will be low, depriving U4 LED of its supply current (R33 through D15) by bypassing it through R34. U4 is a schmitt device only needing R13 pull-up to generate TTL logic levels on the non-isolated side. With the LED unenergised, 'RX-DATA' will be inactive-high. A differential signal (eg RS422) applied to the two receive inputs will cause U4 output to go active low, when RX+ is more +ve than RX-. C13 with R36, R37 provide some noise immunity. R35 gives some 100mV hysteresis. Common mode range is more or less a function of the LM393 supply voltage ie +/- 14 volts. If RX- is left open, its voltage will default to around 1.7 volts. This will be the switching point of an RS232 signal connected to RX+. In this case, however, the input voltage range is extended by D16/D17 which allow R36, R37 to act as a potential divider (about 2:1). +/- 25 volt signals can therefore be accommodated.

Transmit Data:

TX DATA/ from the microboard activates U3 LED (R11, R10, Q3). U3 output (active low - open collector) has pull-up R21 to 7 volts. This 0-7V signal is applied directly to U8-B -ve input. The +ve input is set at 3.5V by R14, R15. R32 is the required "dead" impedance for RS232. The slew rate of the TL071 is typcially 13 V/µS which is well within the maximum specified. The +ve transmit output is routed via R32 for RS232 and R30 for RS422 (485) via the link to TX+. The RS422 (485) -ve output is always connected to TX-.

The latter is unused for RS232. U5 is a 75176, RS422 transceiver, used here only for transmit. The device has its own

internal current limit, but it was decided to impose a lower limit on the device in the event of excessive output loading. Its 5 volt supply is derived from +7 volts through Q6 emitter follower, whose base voltage is set by 5V6 zener D9. Its collector resistor monitors U5 total current, and when this exceeds about 70mA, Q5 conducting start to bring Q4 into conduction, thereby lowering Q6 base voltage, consequently limiting the current drawn by U5. It will therefore be seen that U5 is operating at different levels from the 0-7 volt levels elsewhere. Its two signal inputs, data and enable are converted from one system to the other by R28/D13 and R29/D14 respectively.

5.1.5 RS422 ENABLE Decoding:

The square waveform present at TX1 secondary is converted by R9, C7 to a triangular waveform centred on 0 volts with the peak voltage inversely proportional to frequency. With RS422 ENABLED, the frequency is halved, and the triangle is doubled in amplitude. At the point of peak +ve amplitude is the -ve transition at R9 from TX1 corresponding to a +ve transition on the other side of TX1 centre-tap. The latter signal is converted to +ve polarity only levels by R20/D9 (0-7 volts) and applied to U7-B (D-type flip-flop) so as to clock in its data at the point of peak +ve triangle level. The triangle is compared with a voltage midway between the two alternative peak values (set by R22, R23) by U6-B. With RS422 ENABLE'd (half frequency), (double triangle amplitude), (U6-B output high) U7-B will have log 1 clocked in and U5 is enabled. C12, D12, R26, R27 reset U7-8 at power-up, so as to prevent momentary activation of RS422 transmit during that period.

5.2 Analogue Communications Board (818 only)

5.2.1 Specifications

Operating temperature range:

0-70°C

Power Supplies:

40V + 15%/-5%
5V +/- 10%
-1.2V ref (30ppm)

Input Signal:

Remote analogue setpoint is a -5V to +10V isolated input
Remote input to microboard is a 0 to 1.2V unisolated dc voltage

Output Signal:

Retransmission output from microboard is a PWM signal.
Retransmission is a -5V to 10V or 0 to 20mA isolated output with an accuracy better than +/- 0.5%.

5.2.2 Introduction

This board combines the functions of isolated dc output (max 10 volts range lying between -5 and +10 volts. / 0-20mA, link selectable) and isolated remote analogue setpoint input (max 10 volts range lying between -5 and +10 volts or 0-1.0V between 0.5 and 1.0 volt, link selectable); the two functions are not electrically isolated from each other, but share a common isolated 0 volts. A toroidal transformer is used to transfer power across the isolation barrier. Interface to the microboard is by two logic input signals (to control dc output) and the 0-1.2 volt analogue output signal (controlled by dc in) to be multiplexed to the A to D on the microboard.

One logic input (RETRAN OUTPUT/) is of variable duty cycle to control the dc output level. The other (RESET/) is activated by the micro watchdog circuitry so that during program failure/recovery the dc output defaults to zero volts/current. RESET/ is latched and will only be unlatched by activity on RETRANS OUTPUT/.

5.2.3 Power transfer

Q2 and associated components constitute a blocking oscillator, which functions in the following way: the divider chain R20, R21 ensures that an initial voltage is applied to Q2 gate so that it will conduct. The resulting voltage applied to the transformer primary generates, by transformer action, an increased voltage on the gate, coupled by C11. ie Q2 regeneratively switches on. This is the forward part of the blocking oscillator's cycle. The voltage appearing at the secondary will be 40 volts multiplied by the turns ratio of the transformer. The secondary is centre-tapped and each half is used, thus providing +/-18 volts.

During the forward cycle, transformer primary current increases with time, and will eventually saturate the core. At the onset of this, the voltage drop across R23 will mean that the gate voltage relative to the source is reduced. The result is that Q2 starts to turn off; the action is again regenerative, and the primary inductance causes a flyback voltage to be developed. But because the other end of the primary, now flying positive, is clamped through D5 to the supply, Q2 is protected, since it will be subjected to a maximum of twice the supply voltage. A further benefit is that the stored energy due to magnetisation current is substantially recovered.

5.2.4 Isolated Power Supplies

On the secondary side, D7, D10, C25, C26 generate +/-18 volts. A highly stable 10.1 volt reference is derived from the +18 volt line. The device is U13, a REF01. This is nominally a 10.00 volt reference, but R58 adjusts this by +100mV. Because dc o/p and dc i/p circuits must also function negatively (to -5 volts), a negative reference is also required. U8 (with a gain of -0.51) generates nominally -5.15 volts with the +10.1 volt reference as its input.

5.2.5 DC Output

Data from the micro to control the dc output has the form of a pulse width modulation of non-fixed frequency, but whose duty cycle is varied and trimmed to correspond to the required output. This signal is inverted and buffered by U8-B, before being passed through the +ve edge delay network, R72, R4, C45, D16 and then split into two complementary signals by U8-C & D for driving U10 LED. Turn off time is shortened by the reverse voltage thereby applied, but the remaining 1.5µS difference between turn on and turn off (resulting in a .15% linearity error at 50% span) is nominally cancelled by the turn-on delay introduced by the delay network. U10 is a Schmitt device only needing the addition of a pull-up resistor on the output to recover the digital signal. U7 is a triple 2 i/p analogue switch. U10 output is the control to one section of U7 (B) to switch between the -ve and +ve references. R47, R50, C27, C30 are a filter to convert the PWM signal to a dc level. U7-C is interposed between the two: transparent in normal operation but switching over to zero volts if RESET/ has been latched.

Control circuitry for this section of U7 is also by an opto isolator, U12. Drive for U12 LED is from U14-B, a D-type flip flop which is reset by RESET/, thereby activating U12. This condition can be reversed only by a +ve RETRANS/ edge clocking in logic 1 at U14-B & D input.

The dc signal, applied to the non-inverting input of U9-C, must now be converted to a voltage output or a current output. The output device is Q11, or Q12, depending on the polarity of load drive. Q11 gate (and Q12 base) is pulled up by R70, and pulled down by U9-C, through D14, D15. Q11 source/Q12 emitter current is noise filtered (C31, R59, C35) and voltage feedback, if selected by LK1B, is taken from this point through R55. C37 ensures h.f. stability. The gain of the op-amp/ Q11+Q12 is 1, so after tolerancing the 10.1 and -5.15 volt references, -5->+10 volts output is guaranteed.

If LK1A is selected, feedback for the op-amp is taken from R49. A current (and hence voltage) flows down this porportional to load current. The latter is sensed by R67 in the drain of Q11. U9-B looks for a copy of this voltage across R48, and thereby controls Q8 gate voltage (hence drain/source current). R48 voltage drop will follow R67 voltage drop, and therefore R49 voltage will track load current. The component values are scaled so that 20mA output current gives 10 volts across R49. This load-current-measure circuit functions only for +ve load currents. As such it is also used for +ve current limiting in voltage mode as follows: If R49 voltage exceeds 10.1 volts by 2*Vbe (D11, Q5 base-emitter), feedback current is directly injected to the inverting op-amp input, clamping load current to about +22.5mA.

If the load is to be driven negative, slightly different current control applies. Negative currents (output device=Q12) are sensed in Q12 collector by both Q9 (sense resistor=R66, Q12 current>50μA) and Q10 (sense resistor=R68, Q12 current>5mA); note that for currents greater than 50μA, R66 is bypassed by Q9 base emitter and R60.

In current output mode, the lower current threshold (Q9; >50μA) applies, serving as a virtual clamp on negative currents: Q9 collector can pull the current feedback point (Q8 source/R49 etc) towards the -18v supply, the voltage limit being defined by -18 x R49/(R49+R54) or about -6 volts. R60 reduces the sharpness of the current limit, alleviating stability problems.

In voltage mode, more load current is allowed. Q10 collector current is injected directly into the feedback input of the op-amp via D12/R61. Because very little current is employed, Q10 collector current required to bring about limiting is artificially increased by the addition of R65. This addition necessitates the inclusion of D12.

5.2.6 Remote Input

This circuit accepts a 0-10 volt between -5 and +10 volts input and converts it across the isolation barrier to a 0 to -1.2 volt level for A to D conversion. The principle of operation is that a triangular waveform generated by U2 is compared (U4-B) with a dc level from integrator U6-C, thereby generating a constant frequency, variable duty cycle square wave. This is filtered to a dc level and compared with the remote input level. Any error is integrated by U6 to adjust the squarewave duty cycle. A copy of the square wave is transmitted across the isolation barrier by U11 and converted to a dc level (U5, U1) for A-D conversion.

U2 - Triangle Generator:

U2-C, being in open loop, will be at either +15V or -15V. This is converted to +/- 6.8V by R5/D1.D2 for input to integrator U2-B. If the input is +ve, U2-C + input will have been shifted +ve via R7 (causing the initial condition of U2-C output high) and U2-B will ramp -ve until U2-C + input is pulled -ve through R16, when a reversal takes place: U2-C flips -ve; U2-B integrator input is also -ve; U2-C + input, shifts -ve (+ve feedback) and the triangle changes direction for +ve going. P-P triangle voltage is:

Vp-p = +/-V(D1/D2) x R16/R7
= +/-6.8 x 15/13
= +/-7.5 volts
= 15 volts p-p (approximately)

C7 is included for noise immunity - which might cause false switching of U2-C.

Triangle/error-integrator comparator U4, (output buffer U1):

The triangle generated at U2-B is compared with the output from the error integrator U6-C. R26/C16 are for noise immunity. The portion of the triangle which is more -ve than the integrator level causes U4-B to change U7 Control A from logic 1 to 0, while driving U11 LED. The former causes U7 section A to switch from -5.15V to +10.V. This square wave is filtered to a dc level by R34, C17, R33, C19 to be compared with the input signal at U6-C.

The latter results in an active low signal at the output of U11. This device will exhibit the same turn off delay relative to its turn on time as U10. Because the PWM signal is of constant frequency, the error will be constant and will be taken out by software. Therefore no delay network is needed and U11 output directly controls section A of U5 to switch its output from 0 volts to -1.22 volts. The 0 to -1.22V square wave here present is filtered by R24, C15, R22, C14 to a dc level, and after buffering by U1, is output to the micro board.

Input buffer; Error integrator U6:

The remote input signal is filtered by R12, C9, R17, C13. In some applications, eg where a resistor is externally strapped across the input for conversion of mA signals to voltage signals, a gain of 10 may be required. If LK2B is selected the gain of U6-B will be 10.0. Otherwise this stage is purely a voltage follower.

U6 is configured as a differential integrator. To inhibit ringing of the control loop, derivative ramping is done by C18.

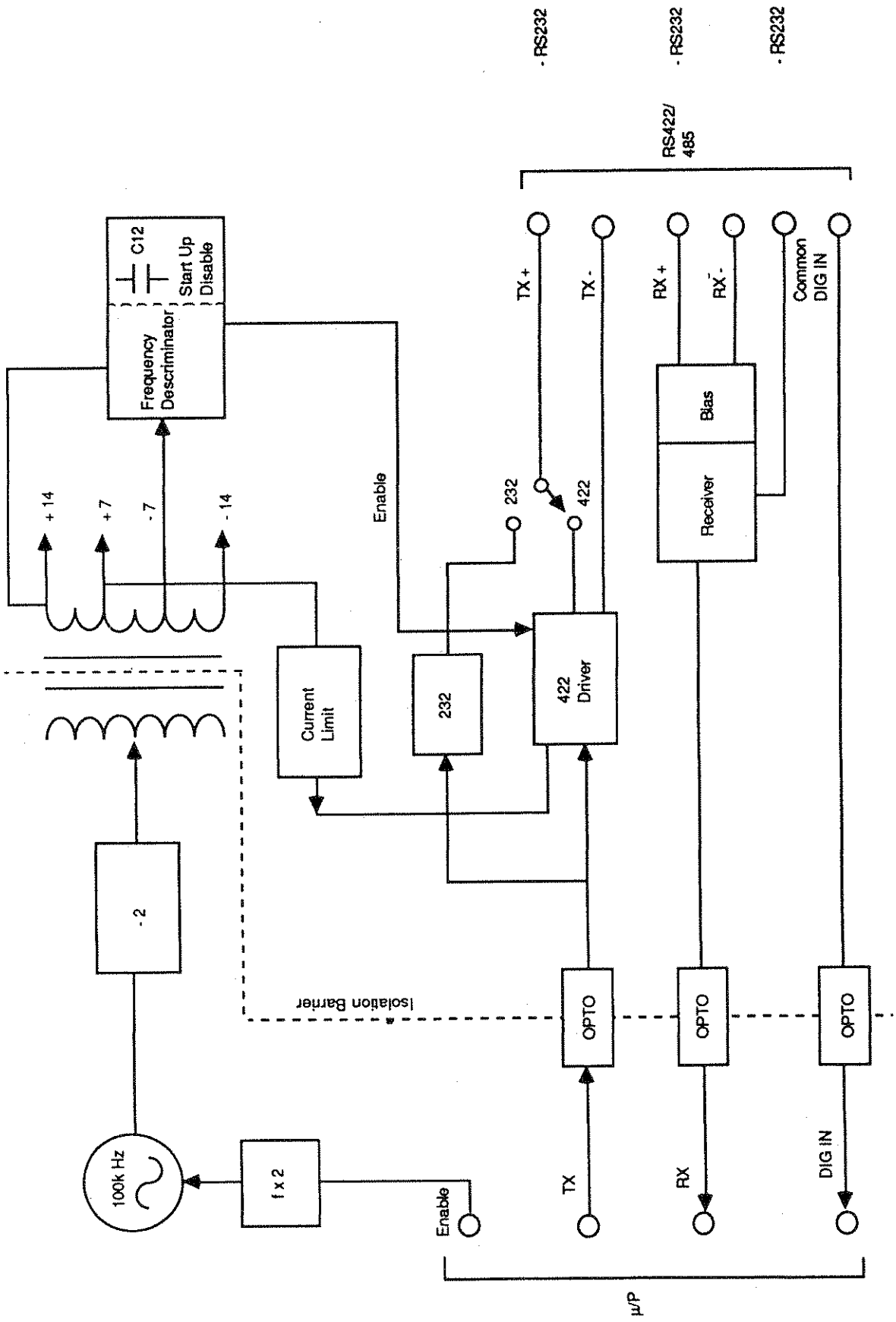


Figure 1 Digital Communications Block Diagram

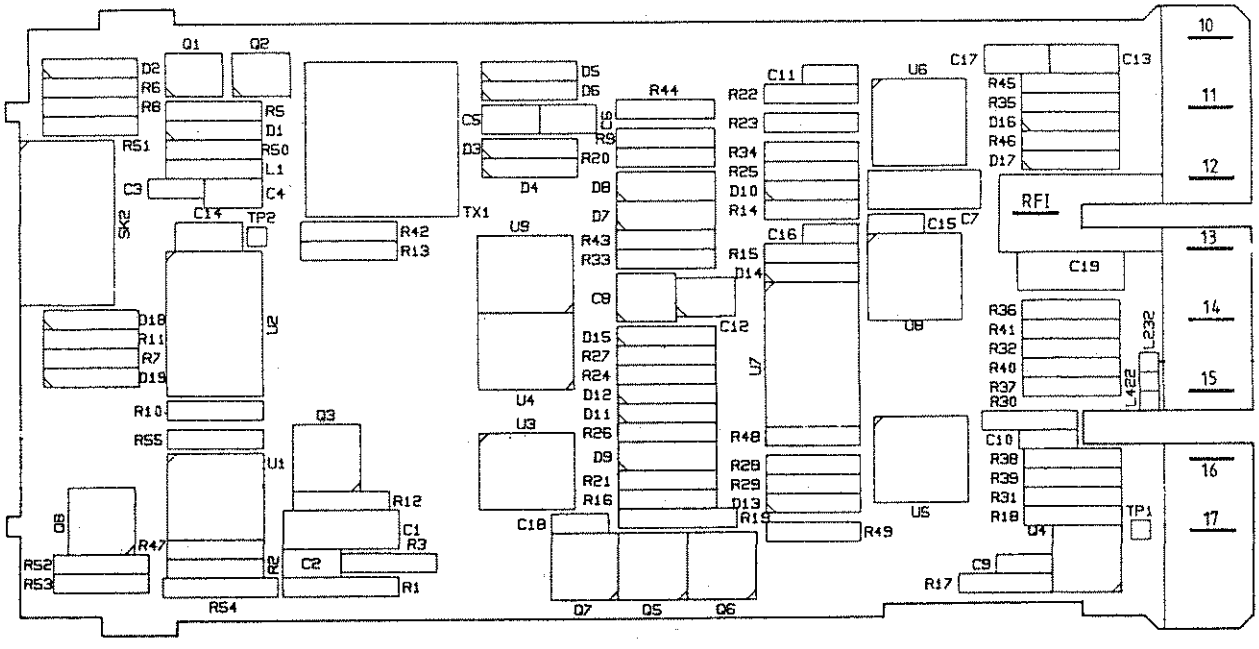
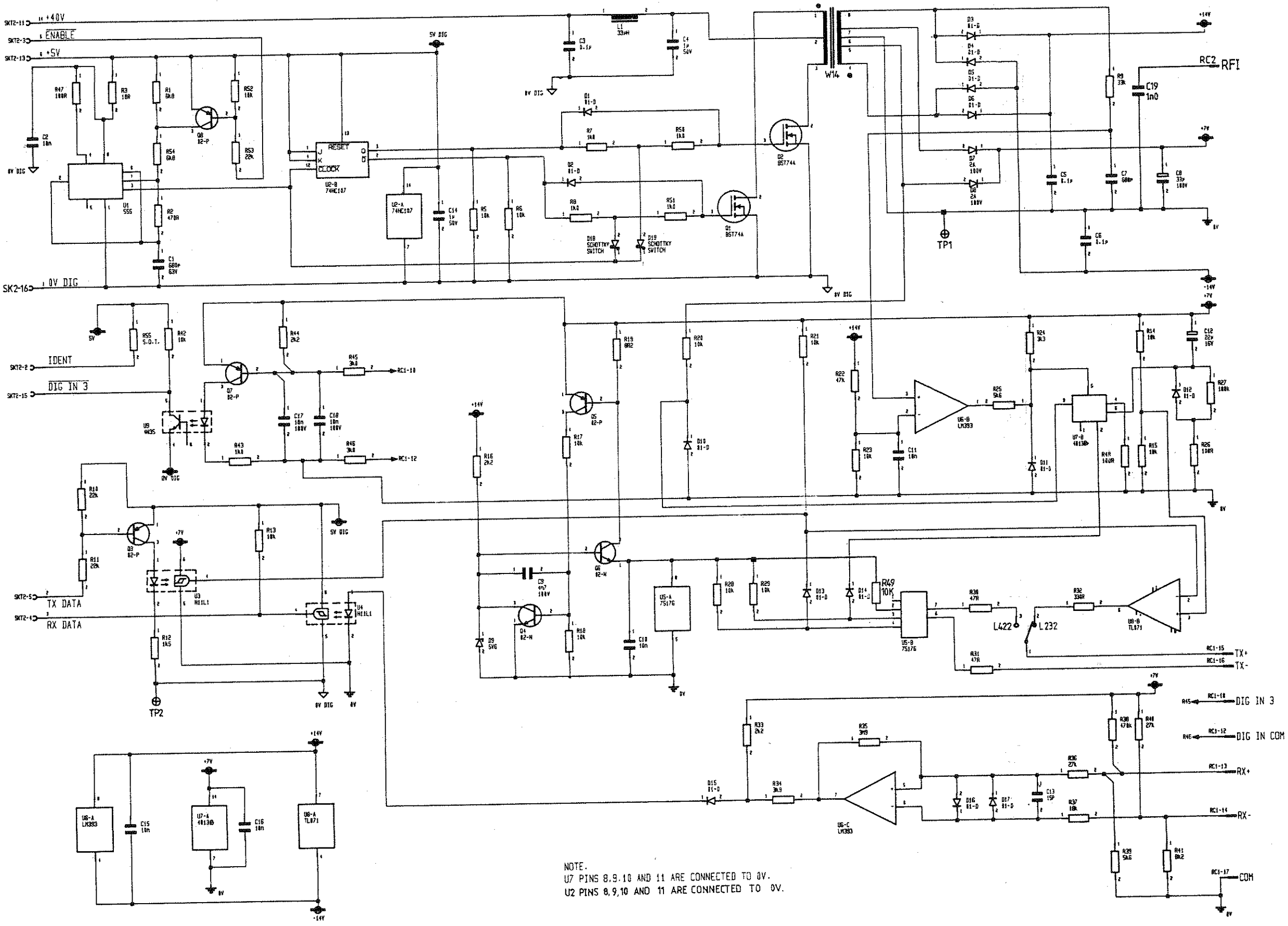


Figure 2. Digital Comms Layout AH020981 Iss 1



NOTE.
U7 PINS 8,9,10 AND 11 ARE CONNECTED TO 0V.
U2 PINS 8,9,10 AND 11 ARE CONNECTED TO 0V.

Figure 3 Digital Communications Circuit Diagram
AI020981 Iss 1

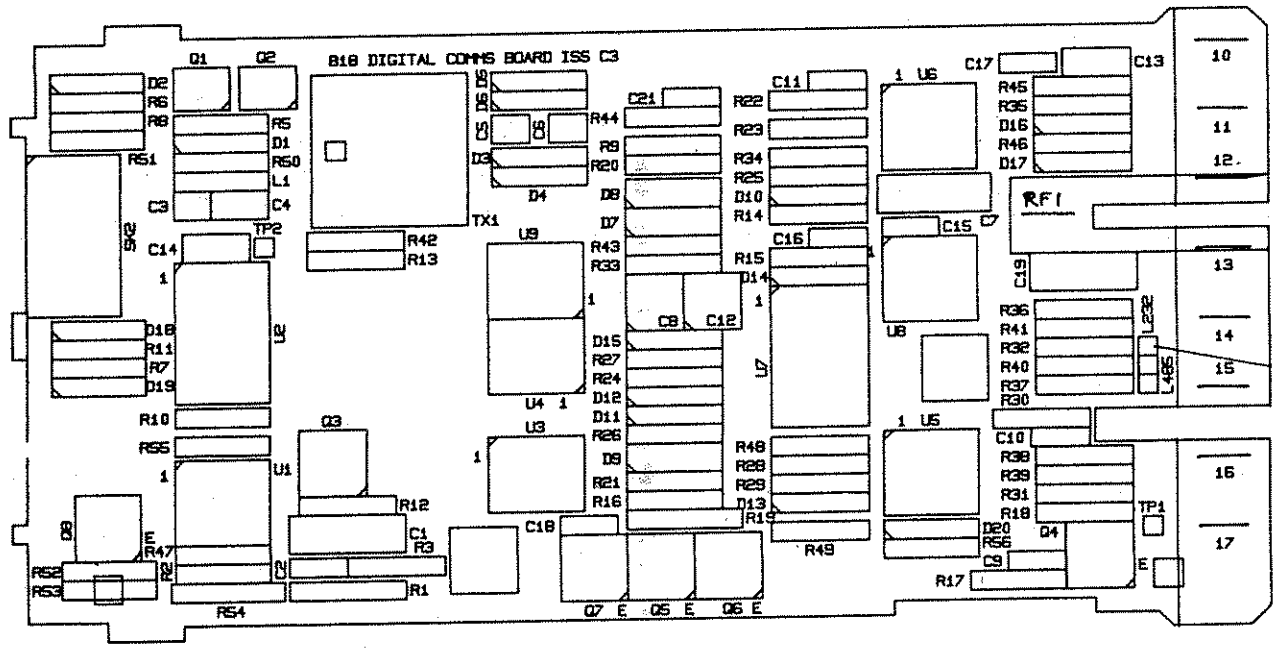


Figure 4. Digital Comms Layout AH020981 Iss C3

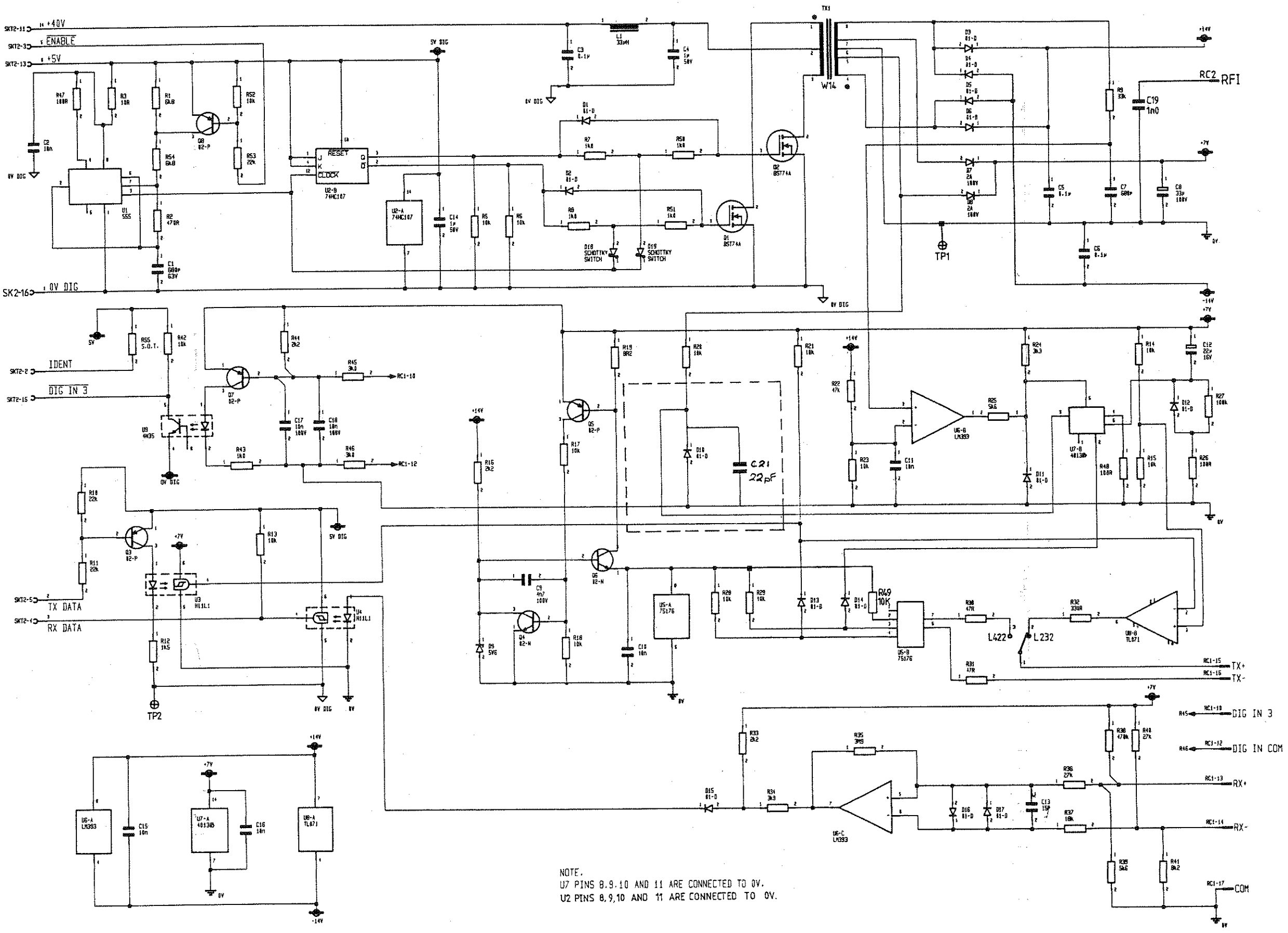


Figure 5 Digital Communications Circuit Diagram
AI020981 Iss 2

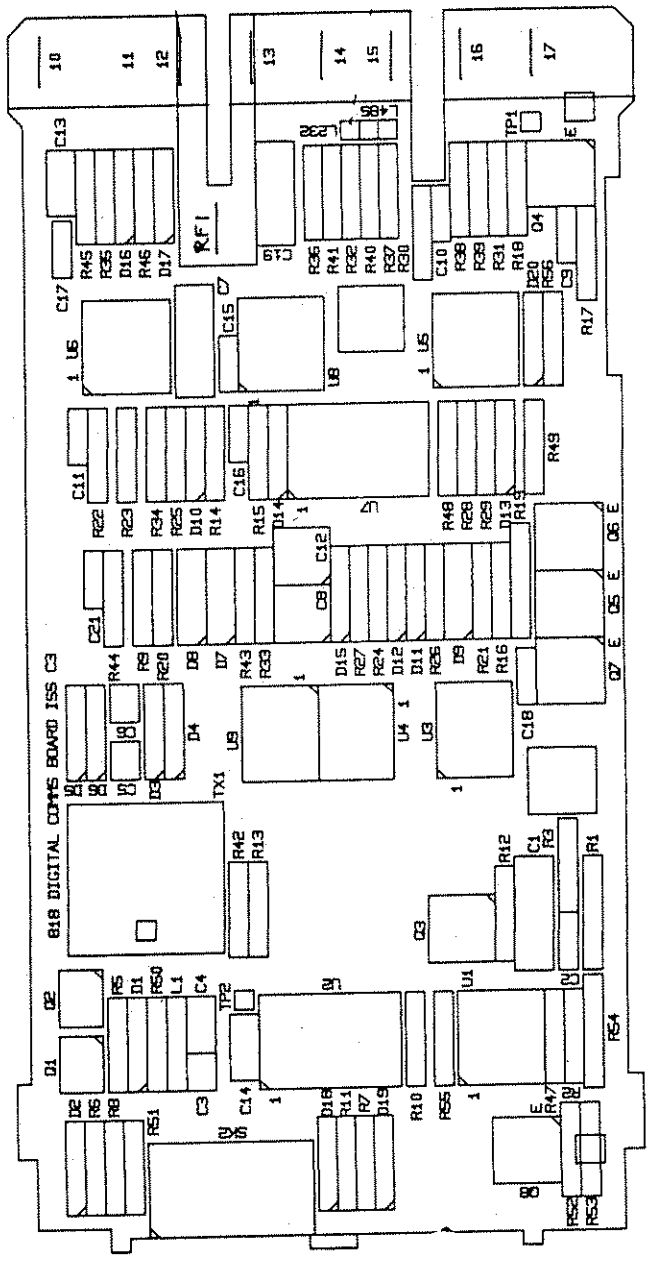


Figure 6 Digital Communications Layout
AH020981 Iss 3

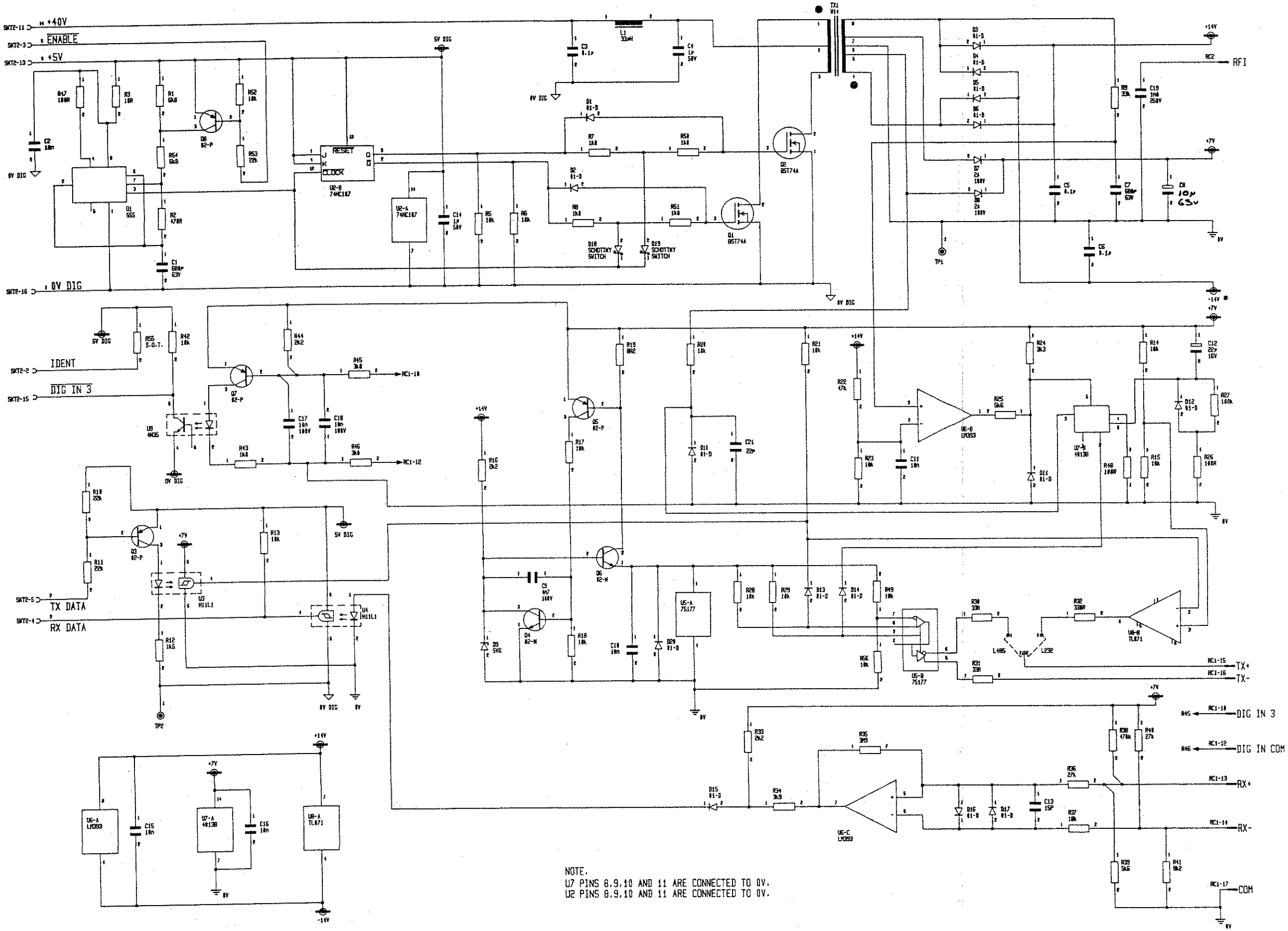


Figure 7 Digital Communications Circuit Diagram
AI020981 Iss 3

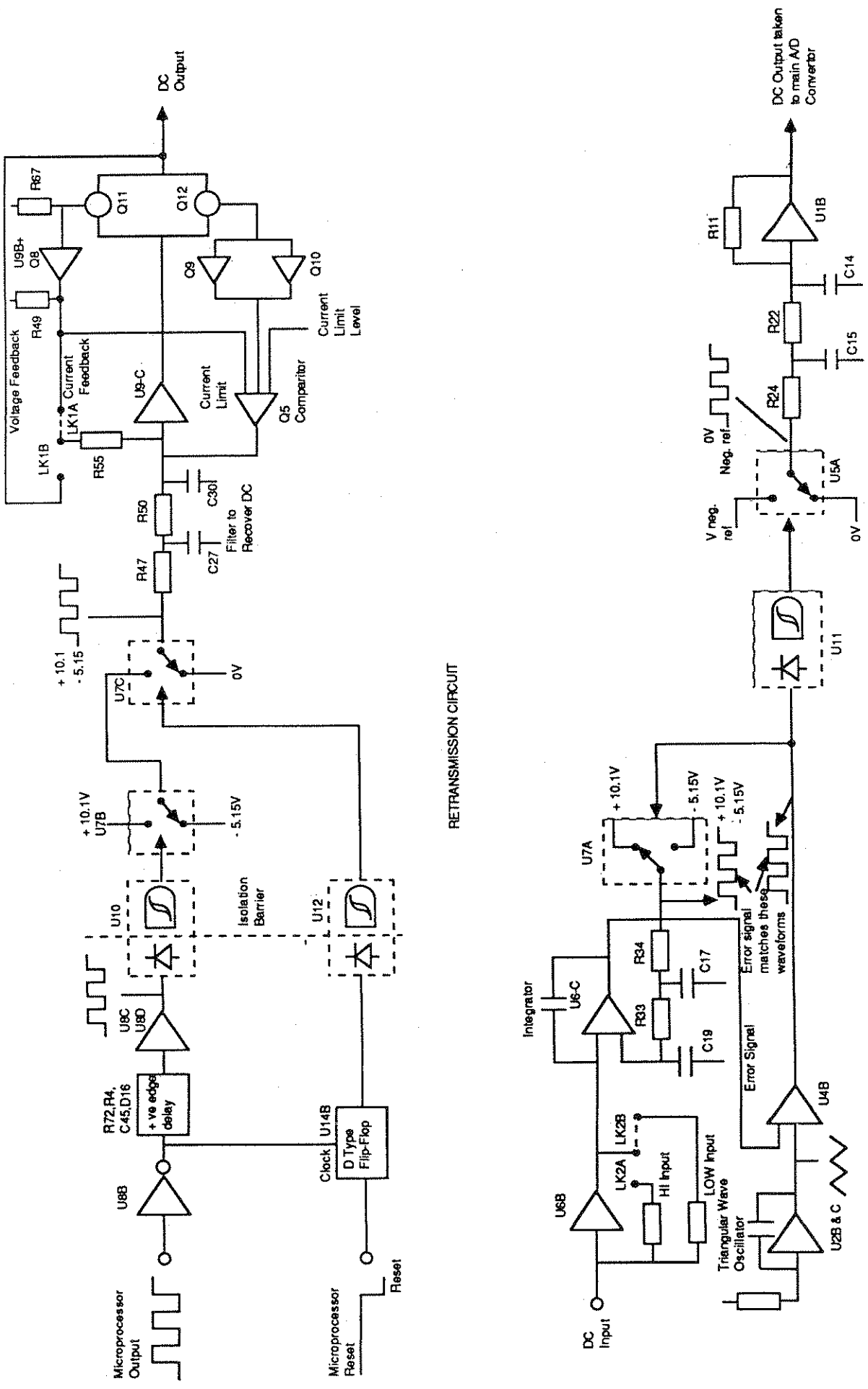


Figure 8 Analogue Communications Block Diagram

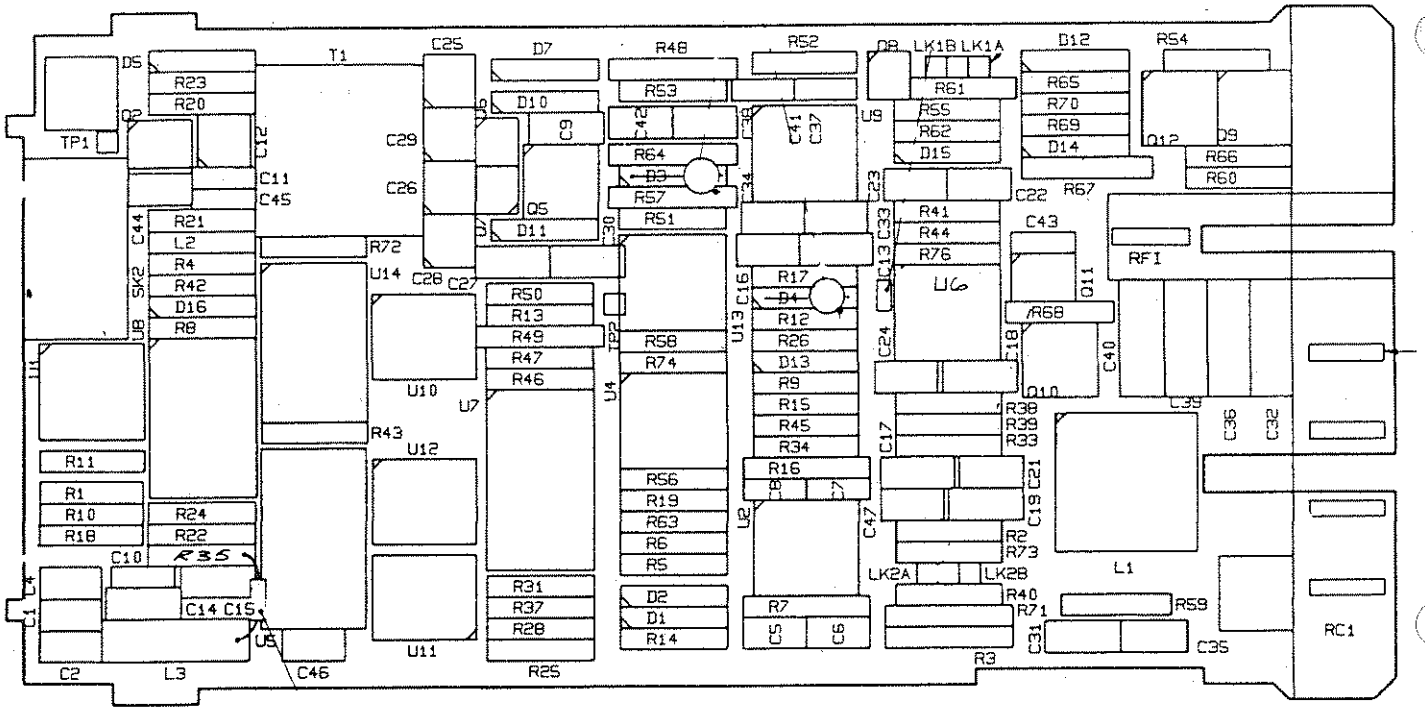


Figure 9 Analogue Communications Layout
AH020992 Iss1

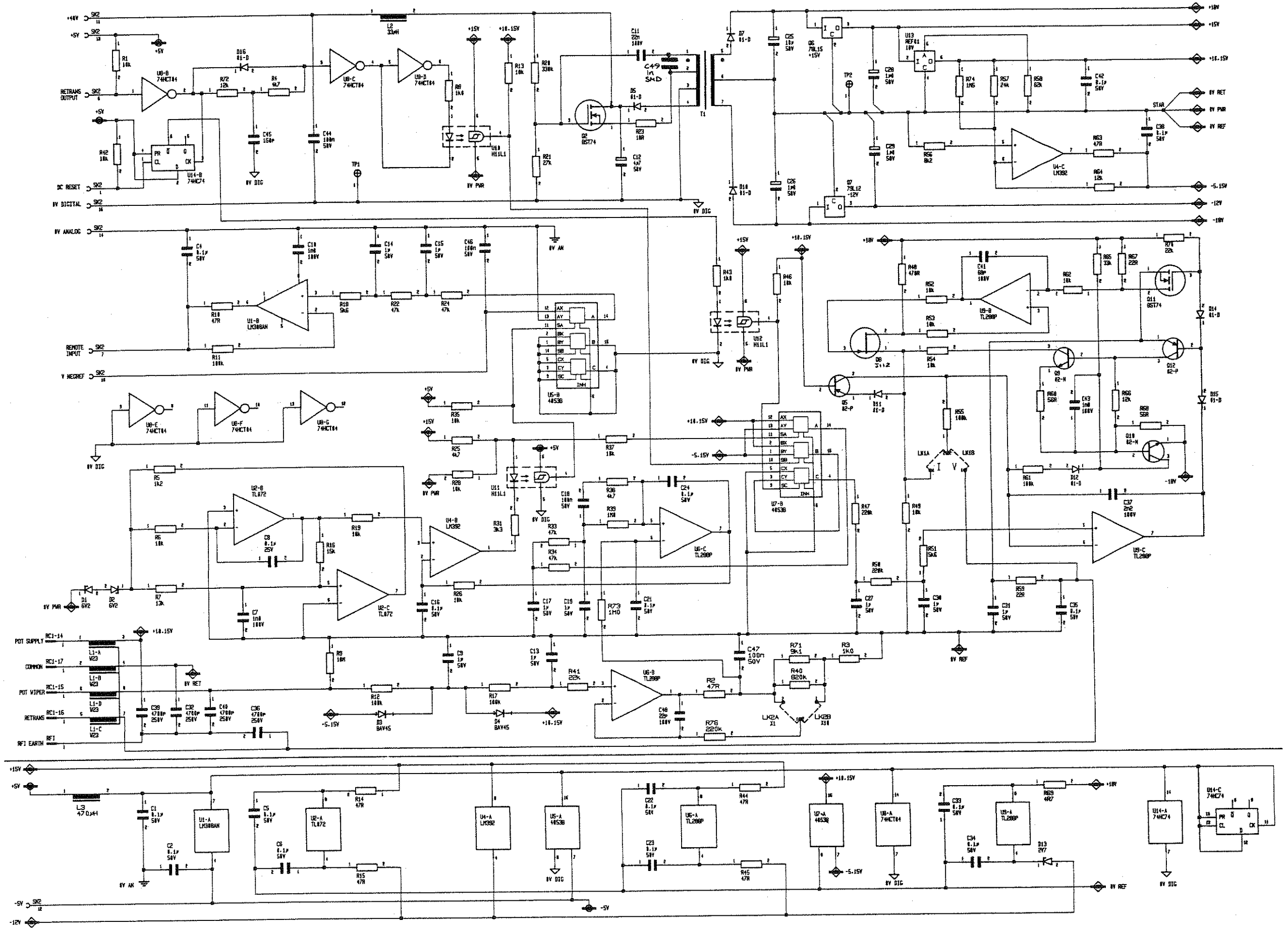


Figure 10 Analogue Communications Circuit Diagram
AI020992 Iss 5

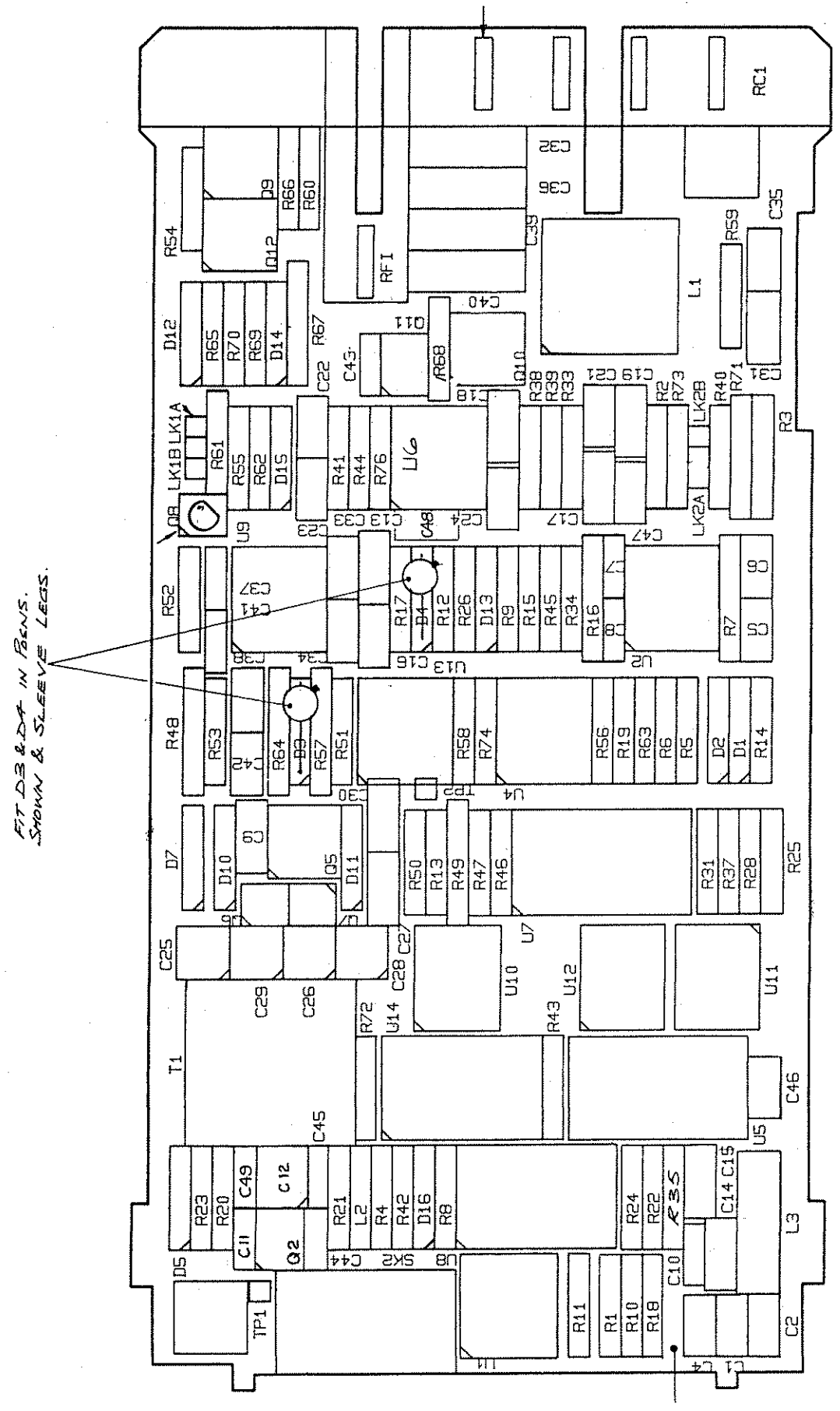


Figure 11 Analogue Communications Layout
AH020992 Iss 4

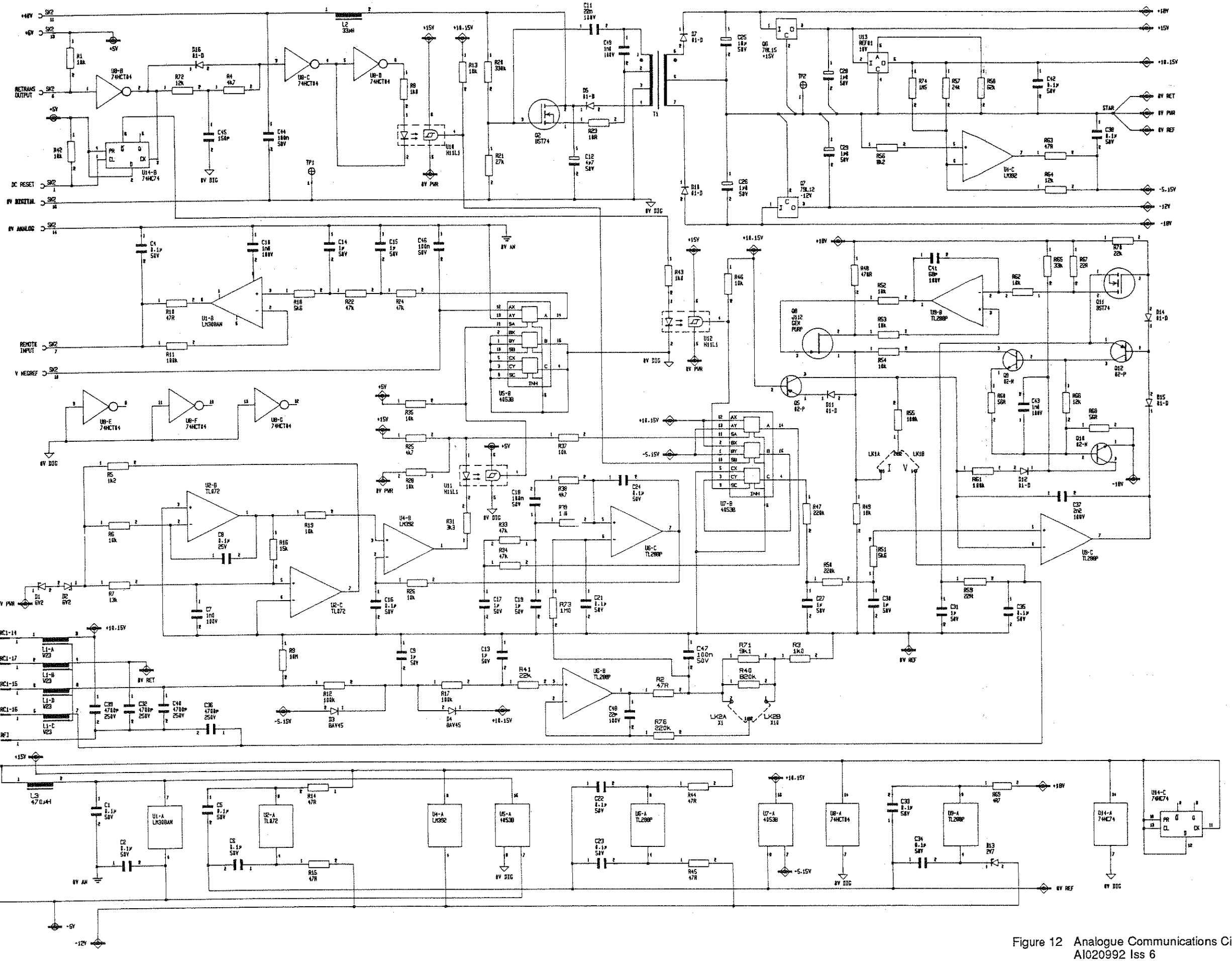


Figure 12 Analogue Communications Circuit Diagram
AI020992 Iss 6

Chapter 6.0 **Display Board**

Contents

6.0 Display Board

6.1 Introduction

Display information is fed to the display board in a serial form. U1-B (75518) is a serial to parallel convertor and also contains line drivers to drive directly into the FIP display DYI.
The display board also acts as a mother board giving interconnections between the various daughter boards in the controller. A heater current limit resistor R1 is also fitted onto this board.
No links fitted.

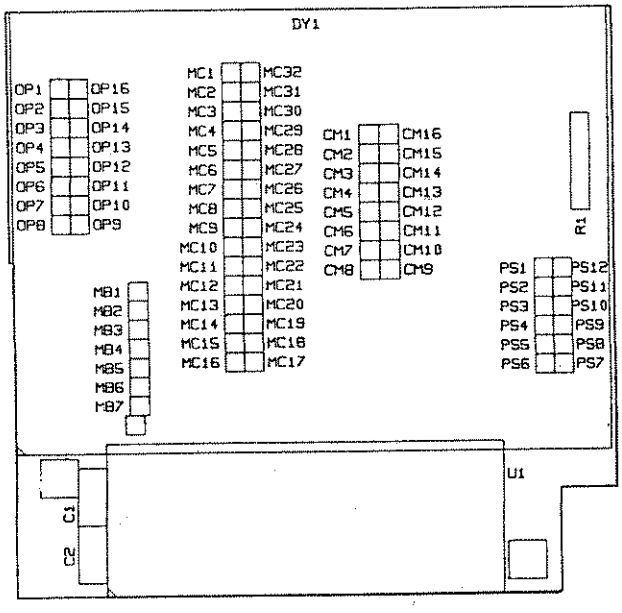
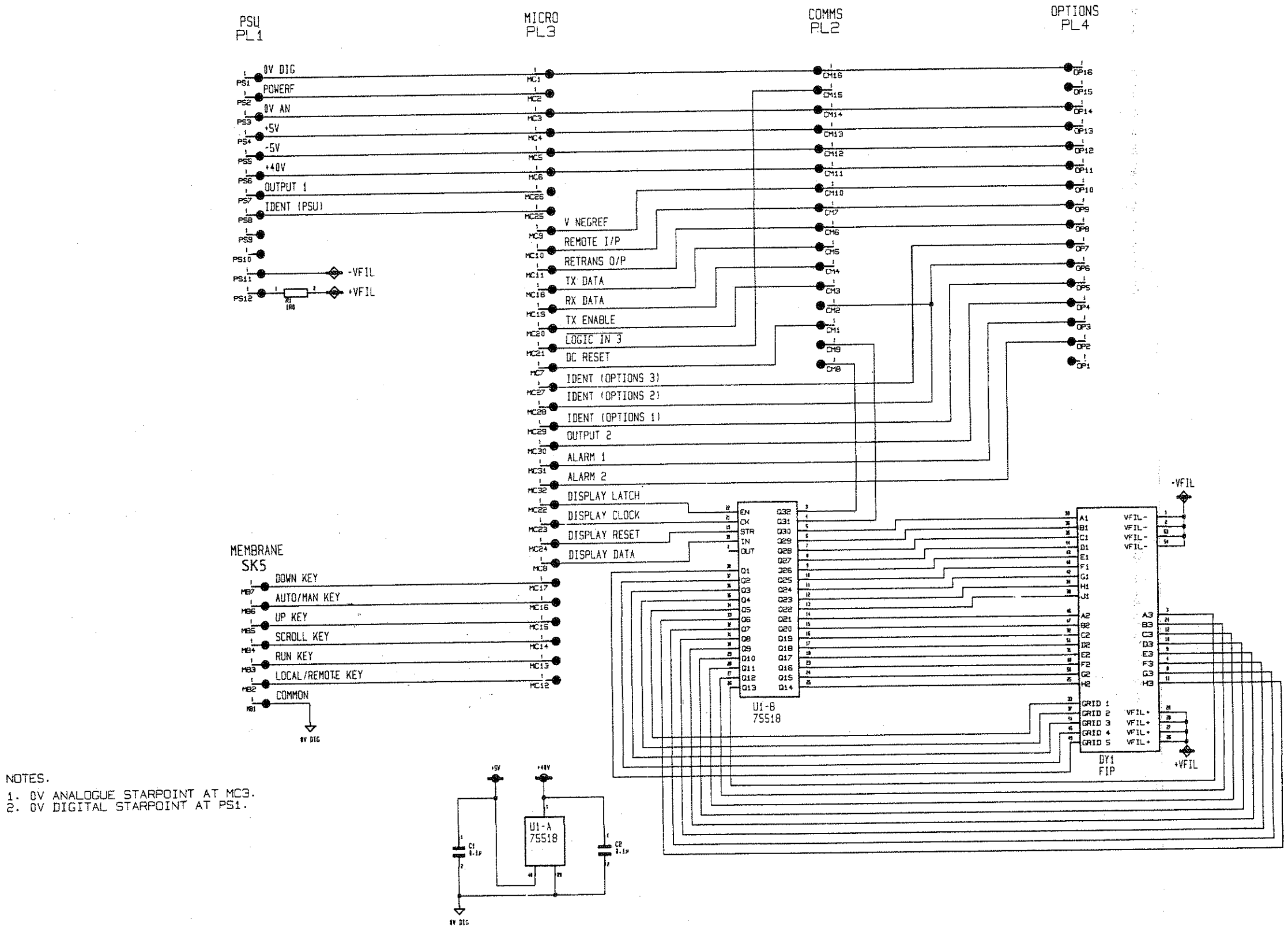


Figure 1. Display Board Layout AI021094 Iss 1



NOTES.

1. 0V ANALOGUE STARPOINT AT MC3.
2. 0V DIGITAL STARPOINT AT PS1.

Figure 2 Display Board Circuit Diagram
AI021094 Iss 1

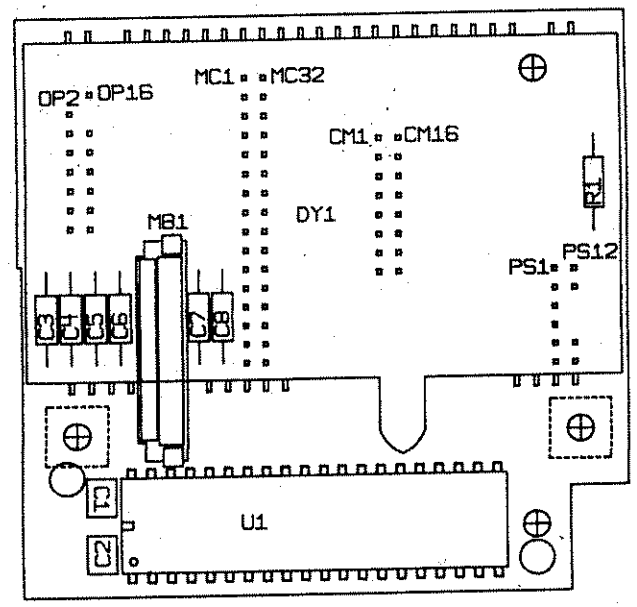
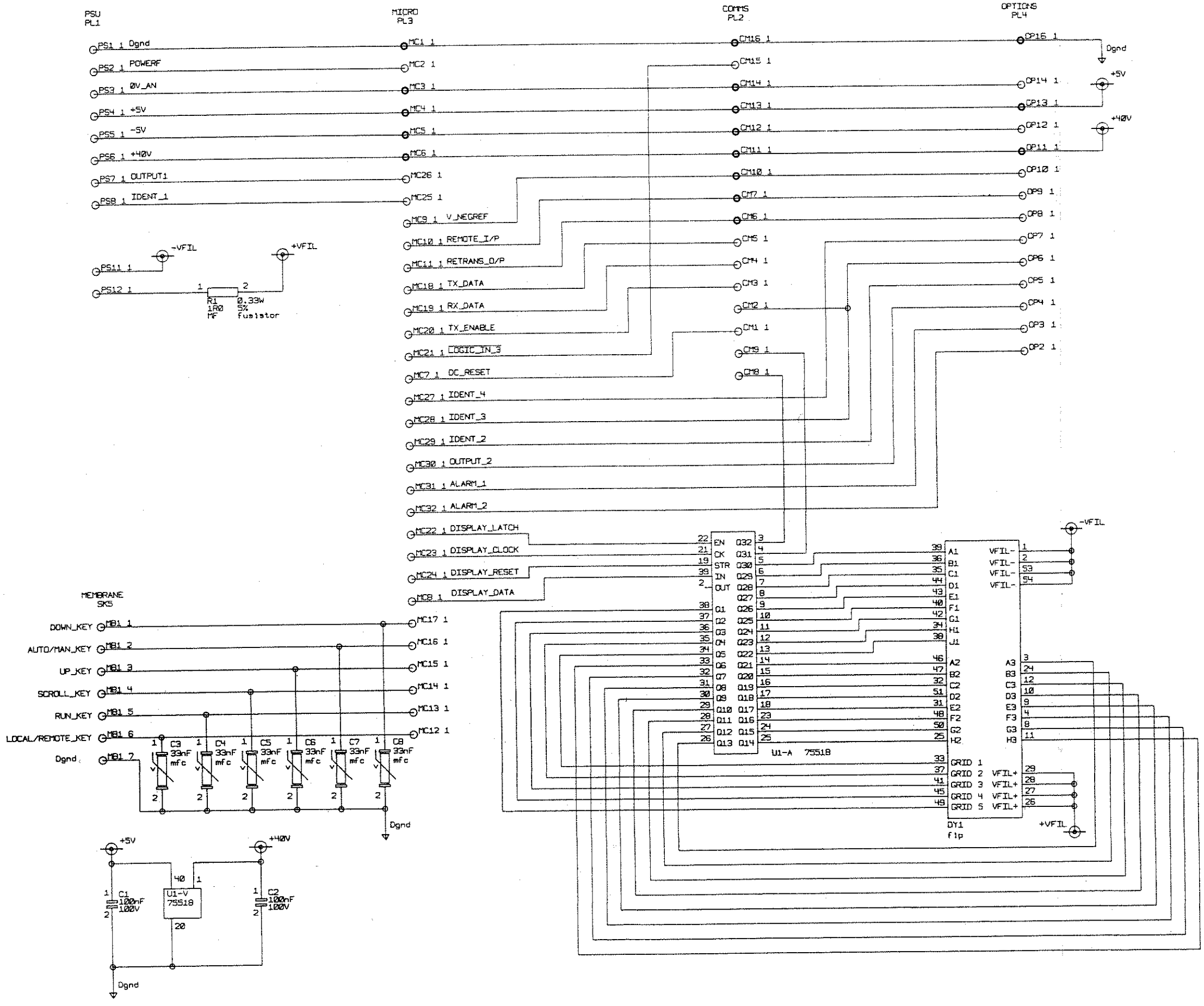


Figure 3. Display Board Layout AH021094 Iss 3



NOTES.

1. 0V Analogue starpoint at MC3
2. 0V Digital starpoint at PS1

Figure 4 Display Board Circuit Diagram
AI021094 Iss 3

Chapter 7.0 **Options Boards**

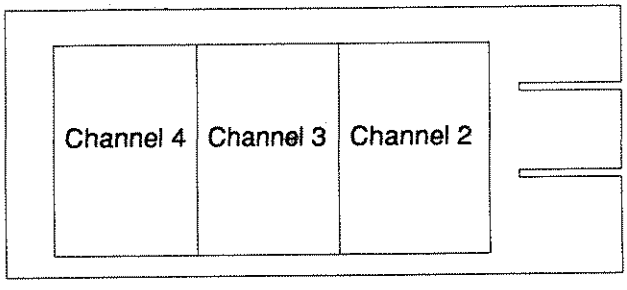
Contents

7.0 Option Boards

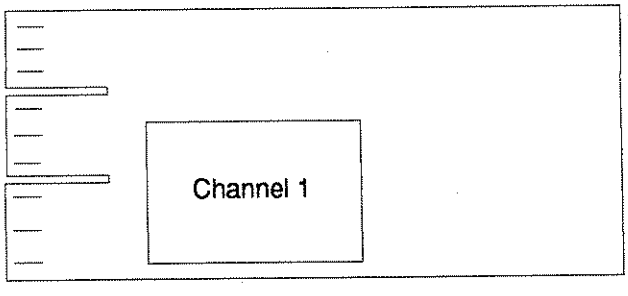
7.0.1 Introduction

The options board is a mother board into which the output 2 module and the 2 alarm output modules (channels 2-4) will fit. Voltage supplies, the drive signal and ident information is picked up from the mother board via the connector and fed to the output modules. The output from the three modules is tracked from the module output connections across to the rear terminal connections. Snubber networks C2, R2 and C3, R3 are also tracked onto this board together with links 2 and 3 for placing these networks across either the normally open or closed relay output. These components which relate to alarm 1 and 2 output (channels 3 and 4), are not normally fitted as snubber networks are fitted to the output modules. In high electrical noise conditions better rejection of noise pick up in to the instrument will probably be achieved by using the snubber networks on the options board rather than the output module.

Options Board AH020988



Power Supply Board AH020979



815 and 818 Options Available

815

Channel 1	2	3	4
Relay Triac Logic DC	Relay Triac Logic DC Retran Remote I/P	Relay	Relay

The instrument can only have one retransmission in output and one remote input, i.e. Analogue Comms or Options modules.

818

Channel 1	2	3	4
Relay Triac Logic DC	Relay Relay Logic DC Retran	Relay Retran	Relay Remote IP VP feedback pot

7.1 Relay Output Board

7.1.1 Specifications

Operating temperature range:

0-70°C

Power Supplies:

40.0V + 15%, -5%
5.0V +/- 10%

Input Signal:

CONTROL - LOW activates relay
0<LOW<1, 3<HIGH<5.25

Output:

Maximum contact resistance 100 milli-ohms (measured at rear terminals)
Minimum switched voltage 30Vdc or 85Vac
Maximum switched voltage 264Vac
Maximum switched current 2A (Resistive)
Settling time better than 300mS.

The relay output module contains a changeover jumper, for the selection of operation of snubber network.

eg; Selection of the snubber network is either normally open, NO, link 1 fitted, or normally closed, NC, link 2 fitted.

7.1.2 Circuit Description

To save power, the relay coil is pulsed at a frequency of about 5KHz with a duty cycle such that the resultant reduced current through it is about twice the dropout value. Although the applied voltage is pulsed, the coil inductance , together with D6, filter the pulses so that the coil current approximate to D.C. The pulse generator is U1-B (1/2 556 Timer I.C.) and associated components. D1 ensures that C2 charge path is only through R5. Discharge path is R6. Duty cycle is thus R5:R6 high going at pin 5. Q2 is driven by this through D2. D2 is present so that a lower frequency pulse signal can also be combined via D5. This lower frequency is generated by the second half of the 556. Its purpose is to ensure security of the on state by applying a longer pulse (greater than the relay pull-in time) periodically. In fact it is about 50mS every second. It is also essential for initial relay turn on. To turn the relay off, both timers are reset (low going) by Q1. This is indeed the circuit's default state, since Q1 is turned on through R1, R2, R3. Only if CONTROL is low can the timers function, commencing with a turn-on pulse from U1-C.

7.2 Triac Output Board

7.2.1 Specification

Operating temperature range:

0-70°C

Power Supply:

5.0V ± 10%

Input Signal:

CONTROL - LOW produces active on state
0<LOW<1, 3<HIGH<5.25 Volts

Output:

85Vac to 264Vac
1A max

Output is isolated to 264 volts and meets IEC 348.

7.2.2 Circuit Description

The solid state relay technique is a lower cost way of implementing triac drive than the more conventional gate-pulse drive method. The triac drive is instead a direct path from Anode 2 to the gate, so that on each half cycle, gate current increases after zero-crossing until the triac Q3 fires, thereby terminating gate drive The control element is U1, an opto-triac, which allows or disallows this gate drive current path, depending on activation of its LED across the isolation barrier. If U1 turns on at other than zero-crossing, Q3 gate current must be limited to a non-destructive value. This is the purpose of R6. It has been anticipated that certain failure modes of Q3 (ie o/c) would cause destructive currents through R6. Accordingly, this is a fusible resistor. To prevent Q3 dv/dt effects spuriously self triggering the device (via Anode 2 gate capacitance) C1 and R5 are a low impedance path to these false gate firing current, which also include U1 leakage current. R9 is a MOV to reduce line dv/dt phenomena reaching the triac Q3 at Anode 2. R7, C2 are a snubber network. And noise immunity is further enhanced by deriving Q3 gate drive current from the junction of these two components.

The LED is driven at 20mA by Q1/Q2 complementary darlington pair, as determined by the logic level on CONTROL from the micro board.

7.3 Logic Output Board

7.3.1 Specifications

Operating temperature range:

0-70°C

Power supplies:

40.0V + 15% - 5%
5.0V +/- 10%

Input Signal:

CONTROL - LOW produces a low output state

0<LOW<1, 3<HIGH<5.25 Volts

Output Signal:

0 to 20mA, 15 Volts min

Nominal load 750R
Slew rate >15 Volts/mS ON and >150 Volts/mS OFF

Output is isolated to 264 volts to meets IEC 348

No links are fitted.

7.3.2 Circuit Description

The function of this module is to convert an active low CONTROL signal into an isolated logic output in excess of 20mA output capability, @>15 volts. The turn on delay is approximatley 200µS; the turn off delay is about 20µS.

Power is transferred across the isolation barrier by a toroidal transformer driven in push-pull by two VMOS devices switching in antiphase. The gate drives are two complementary outputs from a self oscillating 2 NOR gate cross-coupled flip-flop. This works as follows: whichever output is high holds the other output low by cross coupling, and at the same time charges the capacitor on its own input (R1, C1 or R2, C3), until that voltage is seen as logic 1, when the gate output must then go low. Cross coupling ensures that the other gate output becomes high, its input capacitor having been discharged to logic 0 in preparation, thereby confiring the new logic 0 output state of the first gate. The new condition is the converse of the first condition, and will consequently last no longer. The result is an oscillator. At first sight the mark space ratio might be predicted to be greatly dependent on R/C tolerances, until it is realised that the voltage at each RC junction is predominantly dc, of mean level proportional to the duty cycle of the gate output. This effect will self regulate the mark space ratio to typically within 2% of 1:1 with standard components.

The two complementary signals are each gated by the two remaining sections of U1 such that when CONTROL is inactive high, Q1, Q2 gates are both near zero, and the transformer primary has no current through it. To provide a 'dead time' at each transition (a period when neither VMOS is on) as security against a period of simultaneous conduction characterised by excessive simultaneous device current U1-B, C-ve edges (Q1 or Q2 turn-on) are delayed by a RC time contant (R3/C5 or R5/C4). The +ve edges (causing output device turn -off) are not delayed, but are passed to their respective gates by diodes D1 or D2.

From issue 5 PCB the board has been dual tracked to allow use of alternative transformer types.

Generally the transformer secondary centre-tap is connected to isolated zero volts by R17 (zero ohms). It is rectified by D4, D5 to give about 18 volts smoothed by C8. D12, D10 and D11 are not fitted.

Q3 is a linear regulator connected as a switch mode current source. It works as follows: As a linear regulator, there would be 1.2 volts between COMMON and OUT leads, OUT being the more +ve. If L2 were absent, Q3 would control current flow so that R13 voltage drop equalled 1.2 volts. That is, current limit is set by R14 (about 24mA). L2 causes the circuit to switch instead of being linear, since the 1 turn winding applies hysteresis to the 1.2 volt reference. A limitation of the LM317L whereby excessive voltage (about 1.8) applied between C-O, leads to a microsecond or two of non-responsiveness to normal levels, is overcome here by potting down the hysteresis voltage (R14, R16). C11 cures any reluctance to oscillate as a result. The switched waveform is filtered to near dc by L2/C10. D13 is a catch diode, maintaining the load/L2 current path while Q3 is off.

If a negligible load were applied, turn-off of the primary side might not result in rapid turn-off of the output, owing to charge stored on capacitors. To remedy this, a fast turn-off circuit detects the presence of the oscillator signal on the secondary as follows: C7, D3 convert the secondary voltage to -ve going pulses. The amplitude of these is reduced by zener D7. D8 allows the reduced amplitude -ve pulses to charge C9 -ve. In between pulses, C9 will ramp positively (R10, D9) but will never reach zero volts in the available time. On cessation of the oscillator, C9 will become +ve and Q4 turns on, shorting the output to zero volts. This happens within 20µS.

Another undesirable effect with negligible load would be spike rectification leading to an excessive voltage at Q3 IN. Zener D6 cures this problem.

7.4 DC Retransmission Board

7.4.1 Specifications

Operating Temperature Range:

0-70°C

Power Supplies:

40.0V + 15/-5%
5.0V +/- 10%

Input Signal:

CONTROL - Pulse modulated TTL; LOW produces 100% output
0<LOW<1, 3<HIGH<5.25 Volts

Output Signal:

Voltage mode:

0 to 10 Volts, 20mA max

Current Mode:

0 to 20mA, 12 volts min

Nominal load 600R
Accuracy, including linearity 0.5% f.s.d.
Settling time better than 300mS
Input and output are isolated to 264 V meeting IEC 348.

7.4.2 Circuit Description

The purpose of this circuit is to generate 0-10 volts or 0-20mA for signal retransmission. This signal is electrically isolated from the instrument. Both power and data must be transferred across an isolation barrier; a small toroidal transformer generates power; an opto-isolator transfers data.

Power transfer:

Q1 and associated components constitute a blocking oscillator, which functions in the following way: the divider chain R1, R2 ensures that an initial voltage is applied to Q1 gate so that it will conduct, passing current into the primary of the transformer; the gate winding, coupled by C2 applies +ve feed-back, ensuring rapid turn-on of Q1. This is the forward part of the blocking oscillator's cycle. The voltage appearing at the secondary will be 40 volts multipled by the turns ratio of the transformer. The secondary is centre-tapped and each half is used to provide +/-18 volts.

During the forward cycle, transformer primary current increases with time, and will eventally saturate the core. At the onset of this, the voltage drop across R3 will mean that the gate voltage relative to the source, is reduced. The result is that Q1 starts to turn off; the action is again regenerative, and the primary inductance causes a flyback voltage to be developed. But because the other end of the primary , now flying positive, is clamped through D1 to the supply, Q1 is protected, as it will be subjected to a maximum of twice the supply voltage. A further benefit is that the stored energy due to magnetisation current is recovered.

On the secondary side, a highly stable 10.1 volt reference is derived from the +18 volt line. The device is U2, a REF01. This is nominally a 10.00 volt reference, but R10 enables this value to be trimmed to that desired.

Data:

Data from the micro to control the dc output has the form of a pulse width modulation of non-fixed frequency, but whose duty cycle is varied and trimmed to correspond to the required output. This signal is converted to Q3 base drive, to switch current on and off through U3 LED. This is a schmitt levice only needing the addition of a pull-up resistor on the output to recover the digital signal. One section of U4 inverts and buffers this signal so as to switch between 0 volts and its supply, the 10.1 volt reference. The PWM signal is filtered by R12, C7, R13, C8 to become a dc level. This is applied to the non-inverting input of U5-C, and must now be converted to a voltage output or a current output. The output device is Q6. Its gate is pulled up by R21, and is pulled down by U5. If U5 output cannot itself swing to +ve supply, D8 and D11 in between mean that the gate can. Q6 source current is noise filtered (R23/C12) and voltage feedback, if selected by LK2, is taken from this point through R18. C10 ensures hf stability. The gain of the op-amp/Q6 is 1, so after tolerancing the 10.1 volt reference, 0 to +10 volts output is guaranteed.

If LK1 is selected, feedback for the op-amp is taken from R19. A current (and hence voltage) flows down this proportional to load current. The latter is sensed by R22 in the drain of Q6. U5-B looks for a copy of this voltage across R14, and thereby controls Q4 gate voltage (hence drain/source current). R14 voltage drop will follow R22 voltage drop, and therefore R19 voltage will track load current. The component values are scaled so that 20mA output current gives 10 volts across R19. This load-current-measure circuit is also used for current limit in voltage mode. If R19 voltage exceeds 10.1 volts by 2xVbe (D7, Q5 base emitter), feedback current is directly injected into the inverting op-amp input, clamping load current to about 22.5mA.

D9 enables U-5 to give the output a degree of sink capability; but if current mode is chosen, there can be no feedback if the load were to be driven negative. Substantial negative currents could result for near zero output demand. The easiest solution is the removal of LK3 in the diode's path when current mode is required.

Links

2 off convert from current to voltage.

For voltage operation both links LK2 and LK4 must be made.
For current operation both links LK1 and LK3 must be made.

Output Scalers

The module gives a fixed 0-10 volt or 0 to 20mA maximum output.
This has to be scaled in configuration to give the required output on channel 2 (cool)

	Mnemonic c2l	Mnemonic c2h
0-10V	0-20mA	0.0% 100.0%
2-10V	4-20mA	20.0% 100.0%
1-5V	2-10mA	10.0% 50.0%
etc		

For channel 3(Alarm 1) mnemonics are c3l, c3h.
To set these outputs accurately refer to paragraph 20.0 on calibration.

7.5 DC Output Board

7.5.1 Specifications

Operating Temperature Range:

0-70°C

Power Supplies:

40.0V + 15/-5%
5.0V +/- 10%

Input Signal:

CONTROL - Pulse modulated TTL; LOW produces 100% output
0<LOW<1, 3<HIGH<5.25 Volts

Output Signal:

Voltage mode:

0 to 10 Volts, 20mA max

Current Mode:

0 to 20mA, 12 volts min

Nominal load 600R
Accuracy, including linearity 0.5% f.s.d.
Settling time better than 300mS
Input and output are isolated to 264 V meeting IEC 348.

7.5.2 Circuit Description

The layout of the D.C output mode is shown in figure 23 whilst the circuit diagram is shown in figure 24.

This module is a cheaper, less accurate version of the 'retrans module'. The isolated output can be either voltage or current, as selected by 2 jumper links. Voltage output is 0 to +10V; current output is 0-20mA.

Power is transferred across the isolation barrier by a small toroidal transformer. Data from the micro to control the d.c. output has the form of a pulse width modulation of non-fixed frequency, but whose duty cycle is varied and trimmed to correspond to the required output. This data is also transferred via the transformer.

Non-Isolated Side
Q3 and associated components constitute a blocking oscillator, which functions in the following way: the divider chain R4, R5 ensures that an initial voltage is applied to Q3 gate so that it will conduct, passing current into the primary of the transformer; D3 is forward biased and merely exhibits a forward diode voltage drop. The gate winding, coupled by C3 applies +ve feedback, ensuring rapid turn-on of Q3. This is the forward part of the blocking oscillators cycle. The voltage appearing at the secondary will be 40 volts multiplied by the turns ratio of the transformer. The secondary is centre-tapped and each half is used to provide +/-18 volts.
During the forward cycle, transformer primary current increases with time, and will eventually saturate the core. At the onset of this, the voltage drop across R6 will mean that the gate voltage relative to the source, is reduced. The result is that Q3 starts to turn off; the action is again regenerative, and the primary inductance causes a flyback voltage to be developed. The other end of the primary, now flying positive, is clamped through D1 to the supply, and demagnetisation current is substantially recovered. Note that during this flyback period, however, the current path is through zener diode D3 (reverse biased) in parallel with inductor L*. For the first 25% or so of the flyback period, the flyback current is greater than L* current, and D3 will conduct. A short duration pulse of amplitude therefore added to the flyback voltage (across one half of the primary), so that it becomes V supply + V zener = 55 volts. The voltage sustained by Q3 is twice this or 110 volts.
The data signal is transferred by removing the effect of D3 or not; i.e. data encoding is carried by the flyback voltage. This is done as follows:
Q2, a P-channel DMOS device, when turned on shorts out D3. Gate drive for Q2 is derived from TI pin 4, whose voltage during the forward cycle will be -40 volts. (D2,C2 rectify and smooth this). R2, R3 are the gate bias chain, such that the gate voltage will never be more than -20 volts.
The inactive high state of CONTROL/ injects current into Q1 emitter, and the resulting collector current pulls away Q2 gate drive. The extra flyback voltage is therefore present when CONTROL/is inactive high.

Isolated Side
Data recovery:
During flyback, pin 7 of the transformer will be +ve . With D3 shorted, the flyback voltage will approximately equal to the forward voltage; i.e. +20V. If D3//L* are not bypassed by Q2, however, the secondary flyback voltage will have superimposed upon it a pulse of amplitude V(D3) x turns ratio = 15 x 26/53 = 7.5 volts. R* and C* damp out self resonance of the secondary; Zener D7 introduces a threshold; R7, C7 very effectively make the circuit immune to noise and waveform spikes. During the superimposed pulse, current is injected into Q4 emitter, and R9 voltage will rise to reset U1-C. Note that the supply for U1 is drawn from +20 volts, shunt stabilised to 8.2 volts by zener D8.
Thus:
CONTROL/inactive high (data=0) -> Q2 off -> high flyback voltage -> reset U1-C.
U1-C Q output is therefore true; it will be clocked into U1-B at the next +ve edge from T1 pin 5 (R12) i.e. the commencement of the next forward cycle. At the same time, U1-C is set again, ready for the next flyback period.

Pulse Width Mod. to Analogue
Data at U1-B is also true; control of analogue is by allowing or removing a fixed current bleed into the virtual earth of an integrator by means of the data signal. The current is -ve, and is determined by R14 and voltage from shunt reference U2 (2.495 volts nominal//0. U2 tends to oscillate without C8. The current bypass path is D10, D11. Note that the allowing (data=1) of R14 current is by logic 0 at D10 anode. Data completment is therefore used D12 during U1-B Q/=low (subtracts from U2 reference voltage across R14), D9 is added (adds to U2 reference voltage). The two diodes are next to each other so as to track thermally.
The output device is Q5; source current is noise filtered by R17, C10. Q5 gate is pulled up by R16 and pulled down by U3 through D14. A degree of sink capability is afforded directly by U3 via D15. Current limiting of Q5 is achieved by current sense resistor R17 turning Q6 on (> .6/22=27mA), removing Q5 gate drive.

U3 Feedback
Load current is returned through load current sense resistor R19; current feedback is taken from this (R18).
For voltage feedback, R19 is shorted by LK2A (R18 can be left in, since with no volts across it, it cannot contriubute to virtual earth current). LK1A is made, and feedback is from the output through R15.

7.6 DC Input Board

7.6.1 Specification

OT 0-70 PS 5V 40V
Input: 0-10V or 0-1V current I/P by external resistor
Output: to A-D 0-8mV
Accuracy: 05%

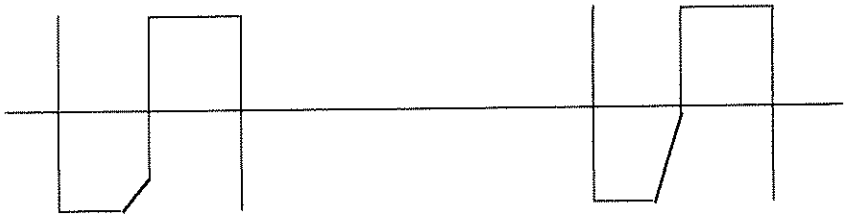
7.6.2 Circuit Description

The layout of the D.C. input module is shown in figure 27 whilst the circuit diagram is shown in figure 28.
This module receives 0 to 1 or 0 to 10 volts (this is isolated from the rest of the instrument; the input range is selected by a jumper link) and conveys information back across the isolation barrier, such that 0 to 8mV is returned to the A to D convertor on the micro board.

Primary Side-Power Transfer
Q4 and associated components constitute a blocking oscillator, which functions in the following way; the divider chain R15, R16 ensures that an initial voltage is applied to Q4 gate so that it will conduct . The resulting voltage applied to the transformer primary generates, by transformer action, an increased voltage on the gate, coupled by C13. i.e. Q4 regeneratively switches on. This is the forward part of the blocking oscillator's cycle. The voltage appearing at the secondary will be 40 volts multiplied by the turns ratio of the transformer.
During the forward cycle, transformer primary current increases with time, and will eventually saturate the core. At the onset of this, the voltage drop across R17 will mean that the gate voltage relative to the source is reduced. The result is that Q4 starts to turn off; the action is again regenerative, and the primary inductance causes a flyback voltage to be developed. But because the other end of the primary, now flying positive, is clamped through D5 and Q3 base-emitter to the supply, Q4 is protected, since it will be subjected to a maximum of twice the supply voltage. A further benefit is that the stored energy due to magnetisation current is substantially recovered.

Secondary Side
The transformer secondary is in equal sections, each generating approximately 7.5 volts. The mid point is isolated 0 volts; one section is rectified and smoothed by D10, C14 to give -7 volts; 2 sections are rectified and smoothed by D8, C16 to give +14 volts. U4 is a 2.495 volt reference fed by R20; D11 in the adjustment lead, adds 1 Vbe to this voltage, anode to cathode. C15 across U4 is essential for H.F. stability.

Data Transfer
Data is transferred in digital form by modifying the flyback waveform from the secondary side and detecting the effect on the primary side. The binary result (a 0 or a 1) is clocked in at each +ve edge of the Power clock, on BOTH sides, so that the analogue implementation on each side is simultaneous. The means of flyback waveform modification is by loading one quarter of the secondary by a 100 ohm resistor during flyback (R19,D9). The resistor value is such that the principle of energy recovery (D5) is not invalidated; MOST of the magnetisation current is still recovered. But with R19 loading the secondary during flyback (switched in by Q5), the flyback voltage decays a lot earlier, somewhat prolonging the flying time; see below:



Normal Waveform Waveform with R19 in circuit

Analogue I/P to Binary Data
A -ve reference current, set by U4 across R21 is either allowed or disallowed by U5-C to flow into the vertical earth of integrator U6-B. D15 in the current path (necessary so that when flip-flop U5-C, Q/ is high no virtual earth current flows) is compensated for by D11 and is physically next to it so that the two diodes track thermally. D11 bias current is 2.495 volts across R34 - the same current as in D15.

R35 is included for the following reason: when U5-C, Q/ is low, D15 forward biased puts 1 Vbe drop across D13, D14 in series. Ideally no current would flow through the series pair, but in practice, and especially at elevated temperatures, a few microamps will flow, constituting an error in R21/D15 reference current. With R35 in the circuit, D14 will in fact be reverse biased by 1 Vbe when U5C, Q/ is low, correcting the error.
+ve current, determined by the d.c. input voltage and the total value of R31+R22+R24 also flows into the virtual earth of U6-B. Note also R23, which adds an offset of about 1 % to allow for input offsets of U6 lest the zero limit governed by the data coding (all 0's) be reached for an actual input voltage greater than 0 volts. The "reference" voltage for this offset is Vbe of Q6, and although this will vary with temperature, the thermal error introduced will be very small. The nominal span voltage (LK2 made, gain =1) is given by:

Vspan/[R31 + R22 + R24] = V[U4]/R21
Vspan = 2.495* 75/18
= 10.4 volts

with LK1 made, the input stage has a gain of approximately 10; the input span is given by:

$$\text{Vspan [gain=10]} = \text{Vspan [gain=1]} * [R31 + R22 + R24]/R31$$
$$= 1.039$$

U6-B output will be continually changing (albeit centred on + 0.6 volts), so that Q6 collector will be continuously switching between high and low. The control loop is as follows: If U6-B tends to +ve, Q6 collector will become low, causing a logic 0 to be clocked into U5-C at the next power clock +ve edge. This results in two things: Q/ output high switches in the 100 ohms resistor for the flyback period immediately following the current forward cycle (to be implemented on the primary side at the NEXT clock +ve edge); and Q output low will be clocked into U5-B to make its Q/ output high - also at the NEXT clock +ve edge. U5-B Q/ high disallows R21 -ve reference current, and leaves only +ve current from U6-C due to the d.c. input, flowing into the integrator virtual earth to cause the integrator output to ramp -ve.

Primary Side- Recovery of Analogue Signal

A normal flyback waveform (no 100 ohms load, corresponding to data = 1) is characterised by the +ve flyback voltage on T1 pin 4 being clamped to the supply by diode D6, and Q3 base-emmitter for practically all of the flyback period. As a result of Q3 base-emitter current, R22 will inject [40V-5V]/R2=1.6mA into the emitter of Q2, and the collector will be pulled up to +5.6 volts. C4 will charge through R5 from a starting voltage of -0.6 volts (clamped by Q1 base-emitter). So long as the voltage on C4 is not being clamped by Q1, Q1 collector current will be zero and logic 1 is present at U1-B D input to be clocked in at the next power-clock +ve edge.

If a zero bit is being recovered, the flyback period starts with the above conditions, but very early on, C4 charge current through R5 ceases, and C4 discharges again via R6, D2. At the next power-clock +ve edge, Q1 base-emitter junction is taking all R6, D2 current, pulling its collector low through R1, and it will be logic 0 that will be clocked into U1-B.

U1-B Q output is the recovered data signal, which is used to supply a current set by R10 into the virtual earth of U2-C. The gain of this device, R11/10, is -0.5454. The output is potted down by R13, R14. For U1-B output switching between 0 and +5 volts, and a duty cycle between 0% and 100% (actually 1% to 97% for a 0 to 10 volt input range), the -mV output will have the limits:

$$0 \text{ to } [5*12/22]*[12/4712]$$
$$= 0 \text{ to } 6.95\text{mV}$$

U1 - B Q Output Voltage

The 4013, although a CMOS device, can have an appreciable drop, even with the light loading in this circuit, between Vdd and it outputs. But to maximise accuracy, Q output must switch between 0 and +5.00 volts. Vdd is derived from the -5 volt supply but use is made of the other half of U1: it is assumed that the output impedance of the two halves will be very similar. The otherwise redundant half is inserted in the feedback loop of U2-B, whose gain is set at -1. U1-C has all inputs tied to zero except SET, which is tied to Vdd/U2-B output. R3, R4 are not only equal with each other, but also with R10. The two Q outputs of U1 are therefore identically loaded. It will be U1-B Q output that is set to +5 volts, not Vdd, which can be expected to be 0.1 or 0.2 volts higher. Because U2 is supplying U1 Vdd, its own +ve supply must be somewhat higher than +5 volts. Accordingly it is taken from the +40 volt supply through zener D11.

7.7 Valve Positioner (818 only)

7.7.1 Specifications

OT - 0-70 PS 5V 40V
Two module positions
MVC Pot feedback circuit
Output 0.5V
Input from pot wiper V12 0-0.5V
output to A-D 1 - 8mV

7.7.2 Circuit Description

The valve positioner board plugs into the option board position in the 818 controller. It has positions for two output modules to be mounted onto it. One of these is for the output module to drive the motor in one direction (channel 2) and can be any of the output modules available. The output module to drive the motor in the opposite direction is situated on the power supply board. The second module position on the VP board is to accommodate a single alarm output module (channel 3).

The circuit components on the VP board are to power an isolated position potentiometer mounted on the drive of the motor to transmit information regarding the position and fault conditions of this potentiometer across the isolation barriers and convert it into a suitable form for presenting to the instruments main A/D convertor.

A block diagram of this circuit is shown in paragraph 18.1 A blocking oscillator Q4 and T1 is used to get the necessary power across the isolation barrier, the insulation between the primary and secondary of T1. The secondary supply is rectified and smoothed in D11, C18 and D9, C17 to produce a -7.5V and a +7.5V supplies. U5.C produces a +5 volt supply from these lines. A +0.5 volt supply for the potentiometer is obtained from U4-C and Q6. The integrator U4-B is alternatively being fed with a +ve current through R29 on a negative current through R19, D14. The switching of this +ve and -ve input is carried out by U3-C. The output of the integrator is compared with the DC value of the potentiometer wiper in the comparitor U5-B. When the output of U5-B goes low, it causes a logic 0 to be clocked into U3-B at the next +ve edge of the power transformer output. This causes Q5 to turn on which presents a low resistance load R20 to the secondary of the transformer during fly back, causing a distortion to the voltage waveform which is reflected through to the primary.

Detection of an open or short circuit potentiometer is performed by monitoring the voltage across the current sense resistor R39. This is performed by U6-B (open circuit) and U6-C (short circuit) which compare this voltage with two fixed voltages generated by R35, R36, R37 and R38. U6-B going high, will cause Q5 to be permanently 'on', U6-C going high will cause Q5 to be permanently 'off'.

When Q5 is 'off' the undistorted voltage waveform on the primary of T1 causes Q3, D4 to conduct producing a charging current for C5 via R5. When the waveform at T1 primary becomes distorted, Q3 and D4 are turned 'off' and C5 charging current stops, turning on Q2 which clocks a '0' into U1-B. This causes the 'Q' output of U1-B to go high providing input current through R6 to U2-C. A DC value is recovered at the output of U2-C from this time proportional input of 1 to 8mV.

General

This valve position module provides an isolated 0.5 volt output for supplying an external potentiometer, and receives 0 to 0.5 volts (eg from the pot wiper) and conveys information back across the isolation barrier, such that 0 to 0.5 volts isolated input returns 1 to 8mV unisolated to the A to D convertor on the micro board.

Primary Side - Power transfer

Q4 and associated components constitute a blocking oscillator, which functions in the following way: the divider chain R16, R17 ensures that an initial bias current is applied to Q4 base so that it will conduct. The resulting voltage applied to the transformer primary generates, by transformer action, an increased drive to the base, through R17, with speed-up capacitor C8. ie Q4 regeneratively switches on. This is the forward part of the blocking oscillator's cycle. The voltage appearing at the secondary will be 40 volts multiplied by the turns ratio of the transformer. The secondary is centre-tapped and each half is used, thus providing +/-7.5 volts. (NB 2 of 4 sections of the W24 secondary are used).

During the forward cycle, transformer primary current increases with time, and would eventually saturate the core. In this design, as soon as the voltage drop across R12 reaches 0.6 volts, further increase in current are prevented as D5, D6 conducts, bypassing Q4 base drive, leading to a regenerative turn-off of this device, and the primary inductance of T1 causes a flyback voltage to be developed. But because the other end of the primary, now flying positive, is clamped through D4 and Q3 base-emitter to the supply, Q4 is protected, since it will be subjected to a maximum of twice the supply voltage. A further benefit is that the stored energy due to magnetisation current is substantially recovered. Reverse base-emitter voltage during flyback is limited by D7.

Secondary Side

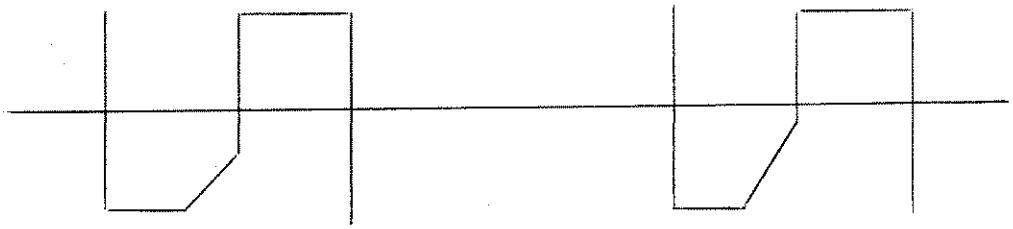
The transformer secondary is rectified by D9, D11 to provide +/-7.5 volts and D15, fed by R21 provides a -2.495 volt reference. C19 across D15 is essential for h.f. stability. A +5 volt supply is derived from D15 reference by U5-C, which is configured to have a gain of -2.

External Pot Supply - +0.5 Volts

U4-C with Q6 emitter follower driven from its output inverts the -2.495 volt reference with a gain of -0.2 to provide a +0.5 volt supply for an external potentiometer. The collector of Q6 is returned to the +5 volt rail through current sense resistor R39 (see below).

Data Transfer

Data is transferred in digital form by modifying the flyback waveform from the secondary side and detecting the effect on the primary side. The binary result (a 0 or a1) is clocked in at each +ve edge of the power clock, on BOTH sides, so that the analogue implementation on each side is simultaneous. The means of flyback waveform modification is by loading one half of the secondary by a 100 ohm resistor during flyback (R20, D10). The resistor value is such that the principle of energy recovery (D4, Q3 base-emitter) is not invalidated; MOST of the magnetisation current is still recovered. But with R20 loading the secondary during flyback (switched in by Q5), the flyback voltage decays a lot earlier; see below:



Normal Waveform Waveform with R20 in Circuit

Analogue I/P to Binary Data

A reference current, set by D15 across R19 is either allowed or disallowed by U3-C to flow into the virtual earth of integrator U4-B. D14 in the current path (necessary so that when flip-flop U3-C, Q is high no virtual earth current flows) is compensated for by D16 which is physically next to it so that the two diodes track thermally. R29 is to give the required offset to the A to D of 1mV. For zero volts input (to U5-B non-inverting), the output of U4-B will be centred on zero. If U4-B tends to +ve, the comparator output will become low, causing a logic 0 to be clocked into U3-B at the next power clock +ve edge. This results in two things: Q output high switches in the 100 ohm resistor for the next flyback period (to be implemented on the primary side at the NEXT clock +ve edge); and Q output low will be clocked into U3-C to make its Q output high - also at the NEXT clock +ve edge. U3-C Q high disallows R19 -ve reference current, and leaves only R29 +ve (zero offset) current to the integrator virtual earth to cause the integrator output to ramp -ve. For zero in, the data average duty cycle will be determined by:

I [R29] = I[R19] x duty cycle
duty cycle = [2.495 x 2/270] / [2.495/18]
= [2 x 18] / 270
= 13%

If the input now receives the +0.5 volts as supplied to the pot (2.495 x 0.2), U5-B comparator must be high most of the time, (keeping the 100 ohm resistor out of circuit and leading to R19 -ve reference current being injected most of the time). For full pot volts on the input:

I [R30] + I [R29] = I[R19] x DUTY CYCLE

duty cycle = {I [R30] + I [R29]} / I [R19]
= {[2.495 x 0.2 / 4.7] + [2.495 x 2 / 270]} / [2.495 / 18]
= {[0.2 / 4.7] + [2 / 270]} x 18
= 90%

Open Circuit / Short Circuit Potentiometer Detection

R39 is the potentiometer current sense resistor: the lower the potentiometer resistance, the greater the voltage drop across R39, and the lower will be Q6 collector voltage; the latter is applied to two comparators - noise suppression being provided by R40, C25. U6-B inverting input is at below +5 volts

5 x [R35+R36] / [R35+R36+R37+R38]

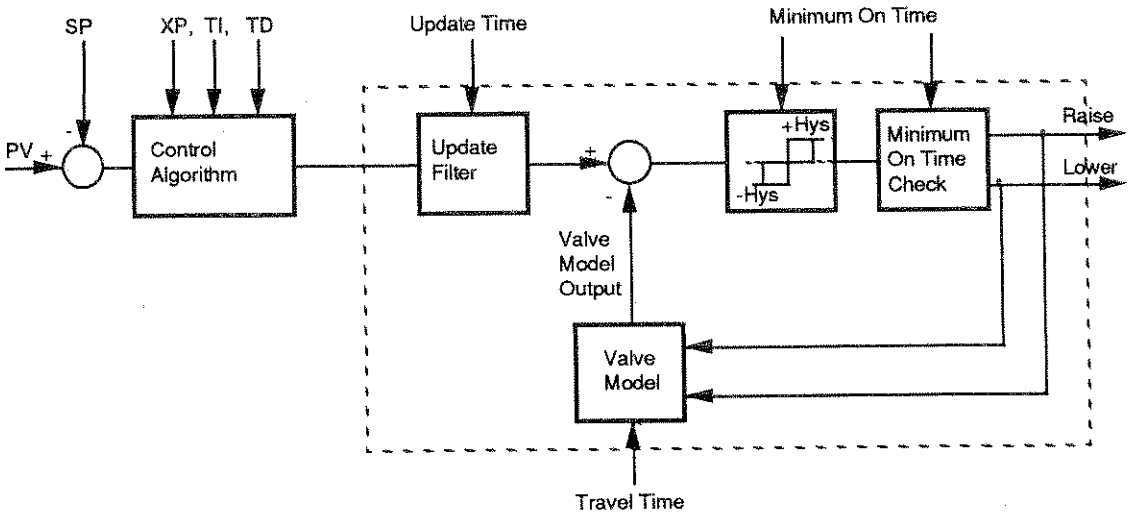
= 5 x [0.56+.082] / [.56+.082+8.2+2.0]
= 0.296

The specified allowed resistance range is 100 ohms to 1000 ohms. For open circuit pots, U6-B o/p will be high, and U3-B will be continuously reset, causing the continuous insertion of the 100 ohm flyback loading resistor - ie data all zeros. The threshold load current is given by:

I load = (0.296 / R39) - (V load / R32)
= 0.296/.56 - 0.5/3.6 mA
= 0.390 mA

7.7.3 Valve Positioner Algorithm

The Valve Positioner is a specialist output for the standard (PID) control algorithm, which pulses triac or relay drives to the raise or lower windings of a motorised valve.



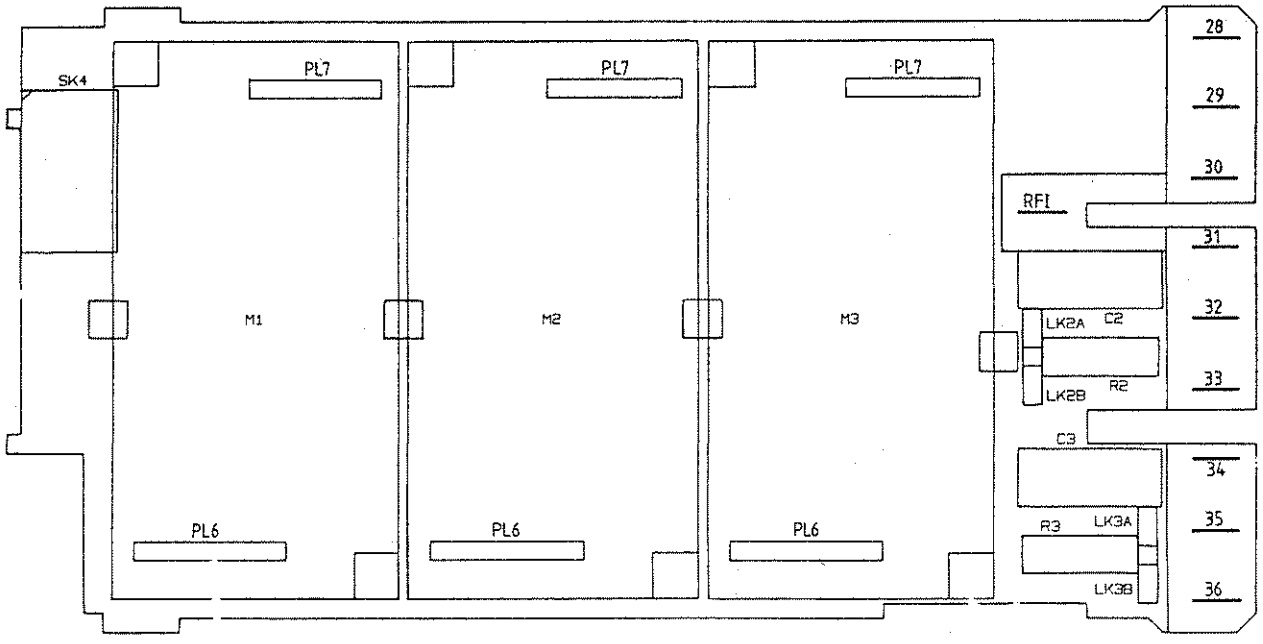
The PID controller demands an output between 0 and 100% from the VP output stage, which simulates the real valve position with a Valve Model. The PID output demand is first filtered and then compared with the output of this valve model. If the filtered output demand is greater than the valve model output, a raise pulse is output to the valve and the valve model output is raised by a corresponding amount. This continues until the valve model output is greater than the PID output. Thereafter, if the output of the valve model is more than that demanded by the PID algorithm plus a given hysteresis, the opposite happens and a lower pulse is output to the real valve, and the model is correspondingly reduced. In order for the model to dynamically track the actual valve output, the motor travel time (between valve fully closed and fully open) must be input to the algorithm, as the time constant of the model. Once either output is off, the error between the demanded output and the model output must exceed the hysteresis before the outputs are re-enabled. The valve model is only approximate and therefore its output does not give an accurate indication of the actual valve position.

The final block of the VP output stage forces the raise or lower pulses to have durations which exceed the minimum on time setting appropriate to the response time of the valve caused by mechanical backlash and motor dynamics. Setting the minimum on time of the output pulses also fixes the minimum OFF time between raise and lower pulses at the same value. The minimum on time is proportional to the hysteresis set in the VP algorithm, which effectively defines an allowable error between model output and PID output during which no output pulsing occurs. The minimum on time is limited to a maximum of 10% of the motor travel time, to avoid too coarse control, as would occur with a large deadband.

Valve activity can be decreased by increasing the minimum on time (and hence the hysteresis), but control hunting will result. The valve update time provides a more effective way of reducing valve activity, by increasing the time between updates to the VP output. For the duration of the valve update time the PID output is summed into a rolling average filter, and this filtered value provides a constant input for comparison with the valve model output, throughout the following valve update interval. As a result, valve activity only occurs at the start of each update time and continues till the valve model output is within one hysteresis band of the filtered PID output.

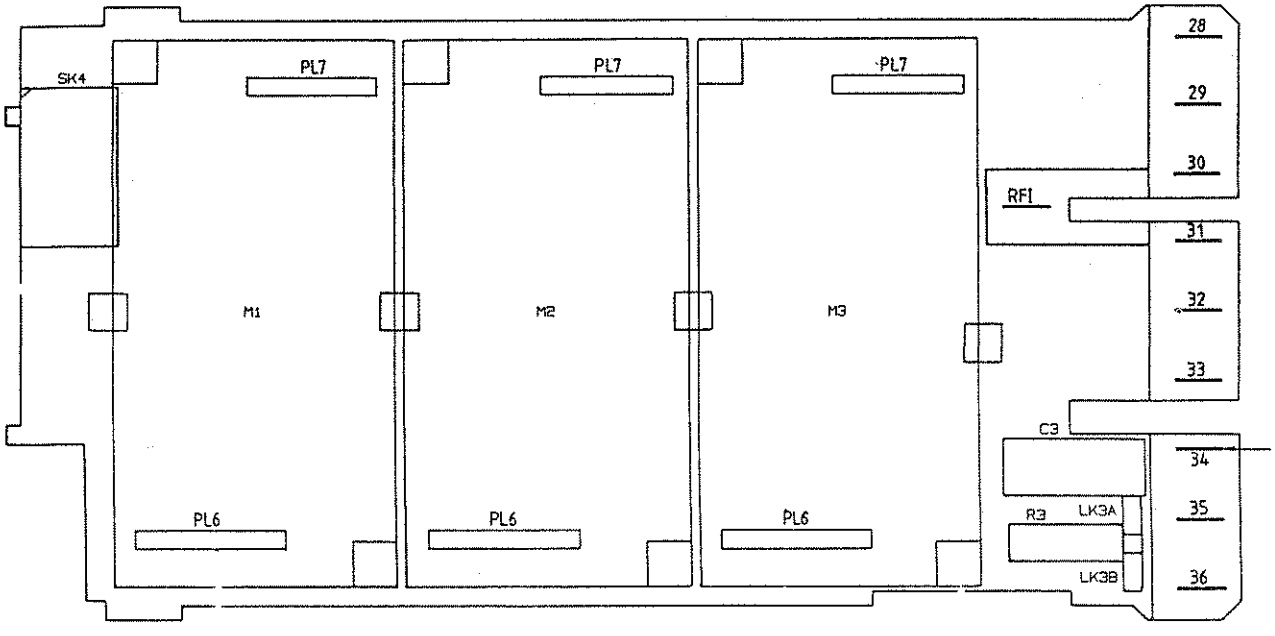
Having defined the motor travel time and minimum on time appropriate to the real valve, it is possible to auto-tune the loop in the normal manner, with the motor travel time appearing like an output rate limit. The PID and cutback parameters all have the same effect as for a standard controller. The valve update time should not be set larger than 1/4 of the derivative time.

If valve position feedback is available, the feedback signal can be displayed and compared with software limits. If the feedback signal indicates the valve position is outside one of these limits, the raise/lower output is disabled simulating a microswitch in the final output drive.



NOTE.
C2, C3, R2, R3, LK2 AND LK3 MAY NOT ALWAYS BE FITTED.

Figure 1. Options Board Layout AH020988 Iss 1



NOTE.
C2, C3, R2, R3, LK2 AND LK3 MAY NOT ALWAYS BE FITTED.

Figure 2. Options Board Layout AH020988 Iss 3

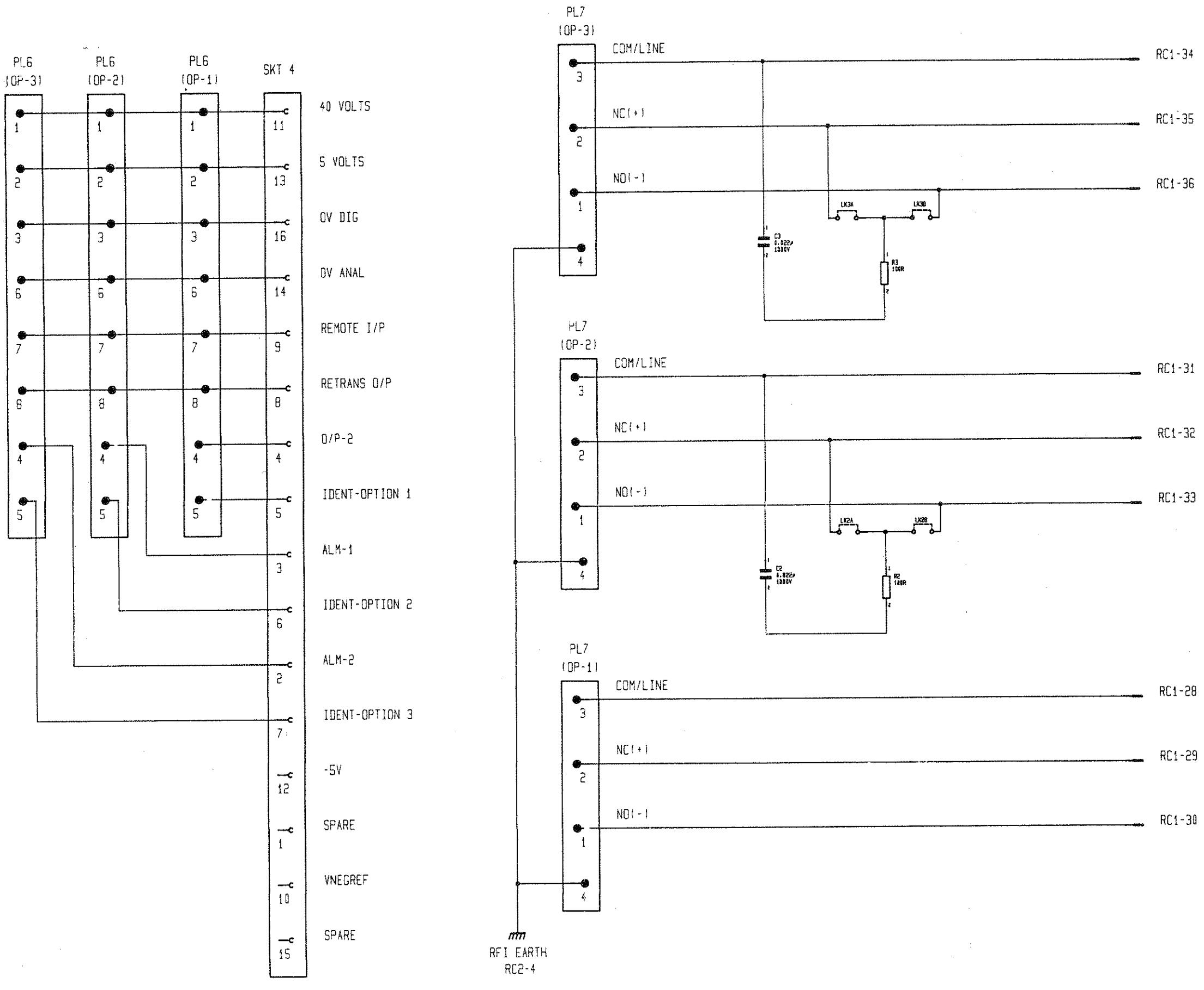
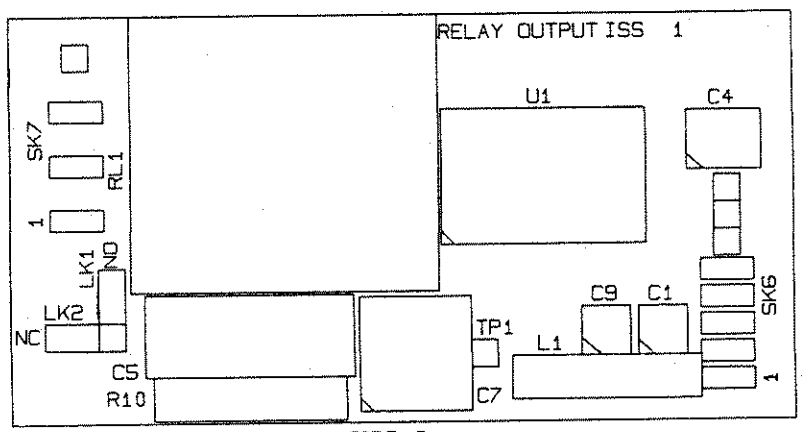
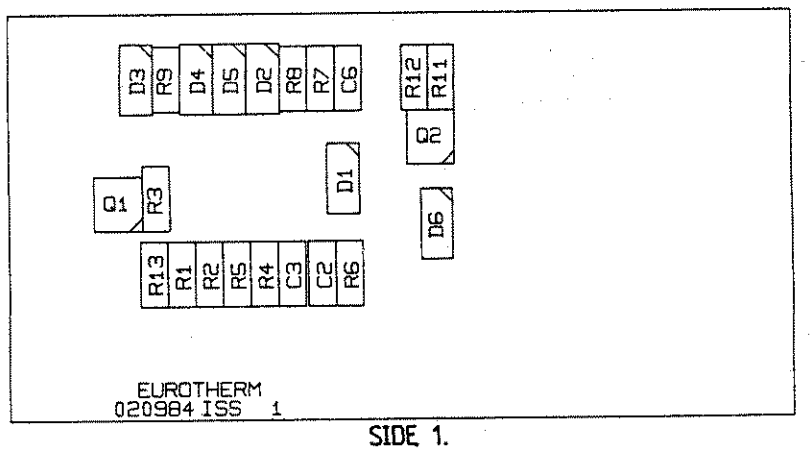


Figure 3 Options Board Circuit Diagram
AI020988 Iss 3



SIDE 2.



SIDE 1.

Figure 4. Relay Output Layout AH020984 Iss 1

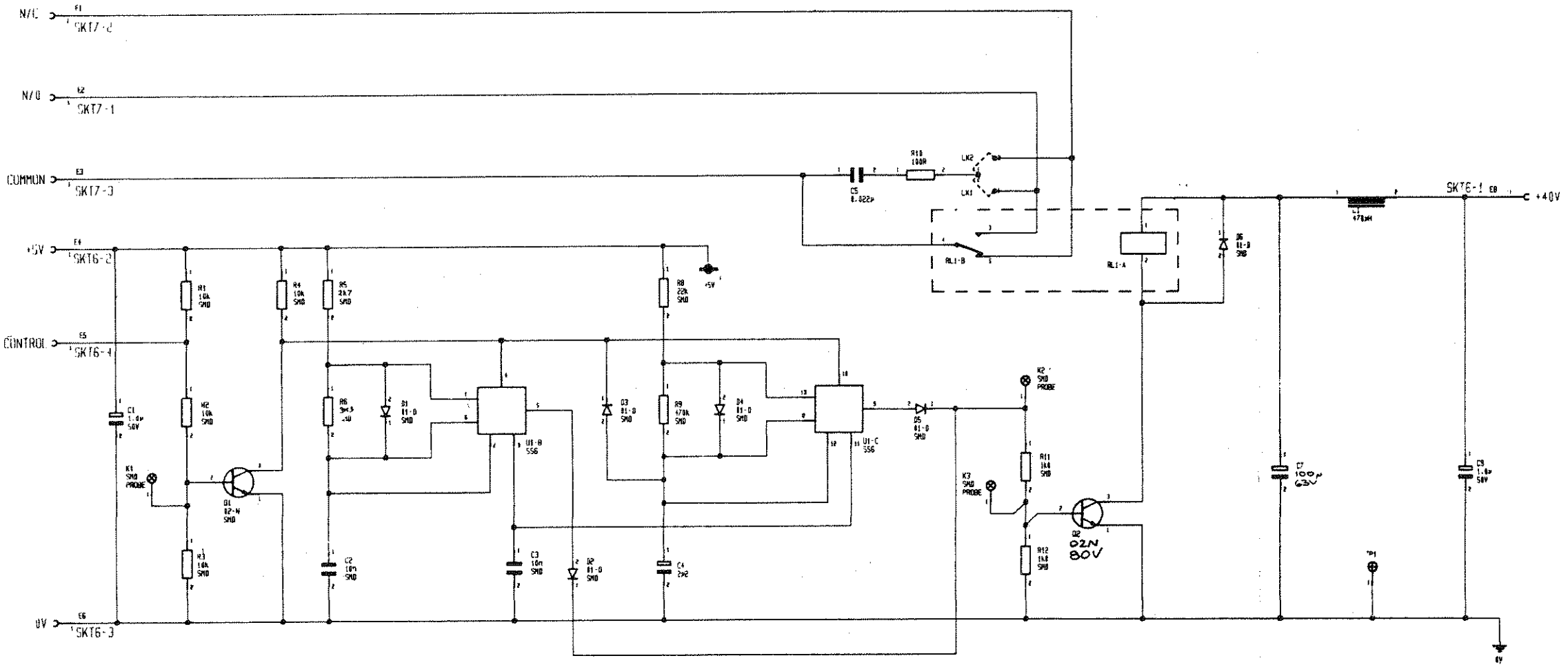


Figure 5 Relay Output Circuit Diagram
AI020984 Iss 3

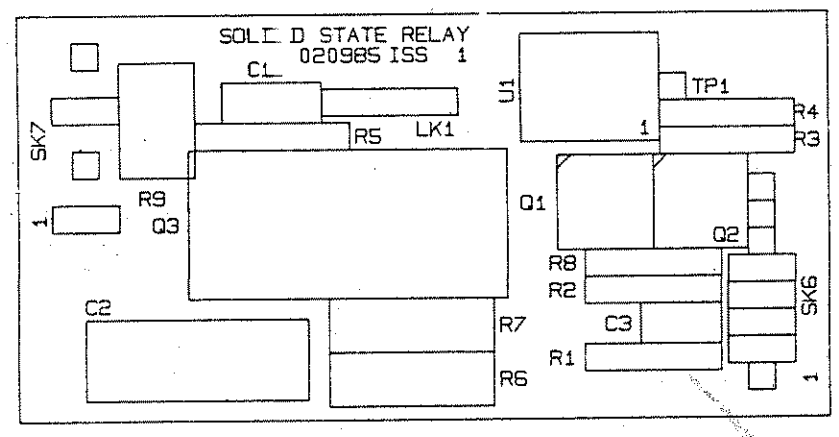


Figure 6. Triac Output Layout AH020985 Iss 1

NOTE:
EUROTHERM APPROVED PARTS INCLUDE:
U1. S21 MD3 (SHARP)
Q3. BTA 10.700B
R6. 1/3W FUSISTOR NFR 25(MULLARD)
R9. MOV-Z280C (POWER SCIENCE)

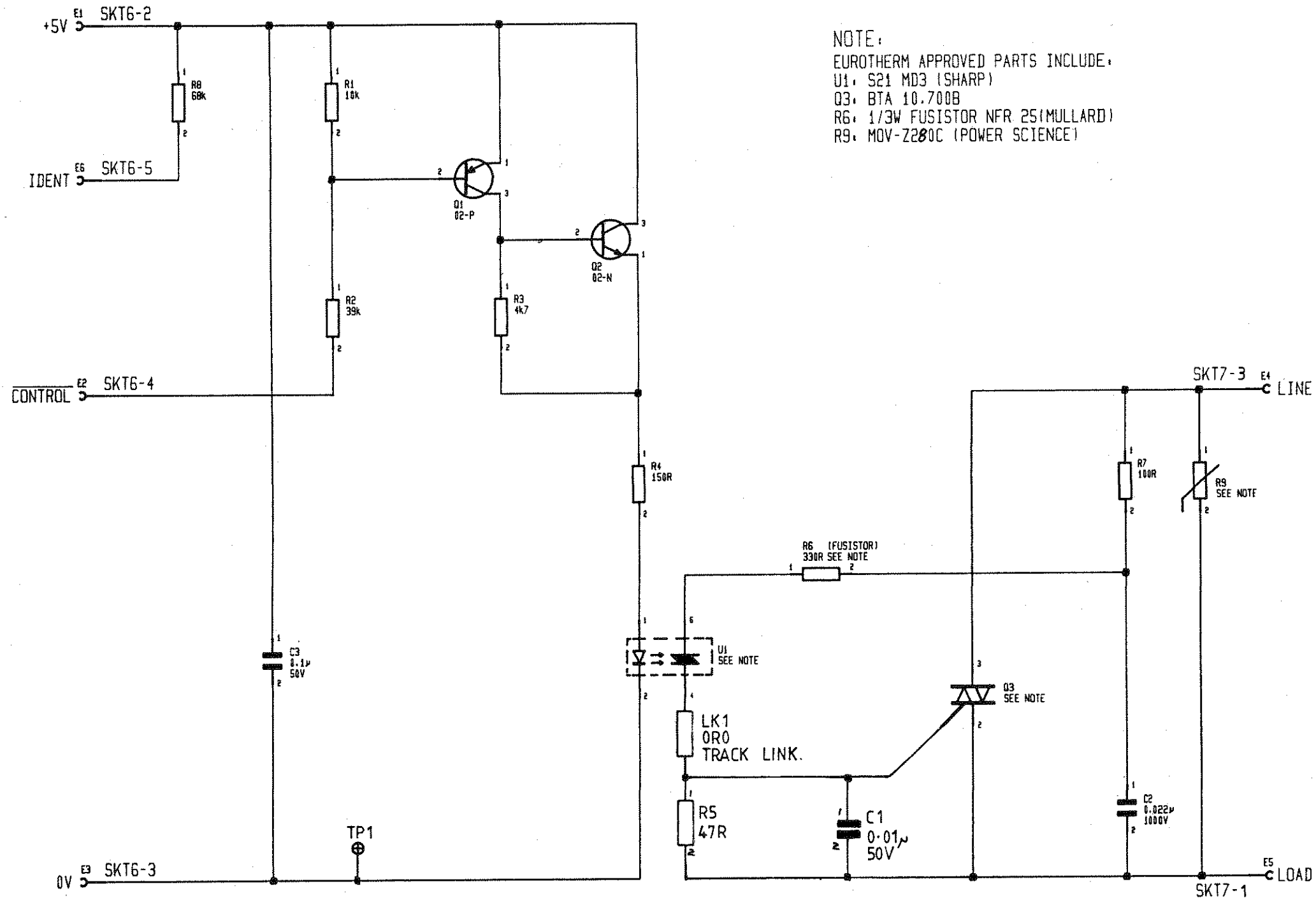
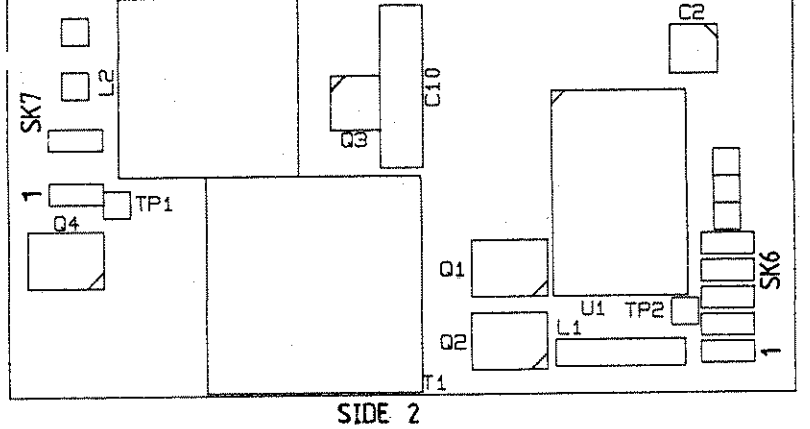
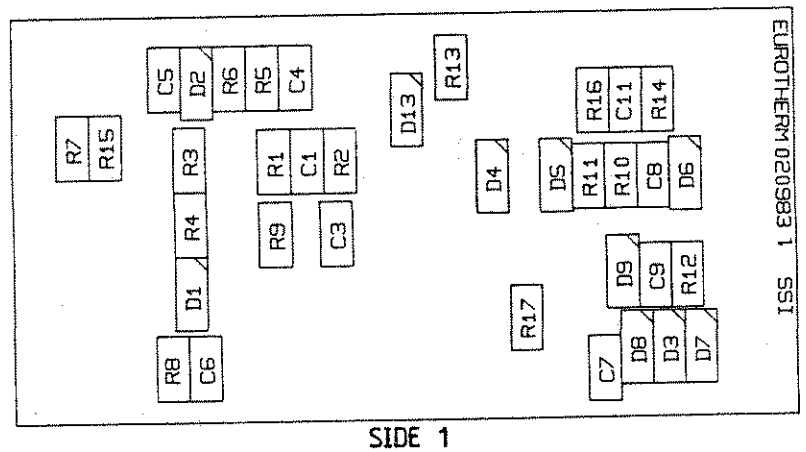


Figure 7 Triac Output Circuit Diagram
AI020985 Iss 2

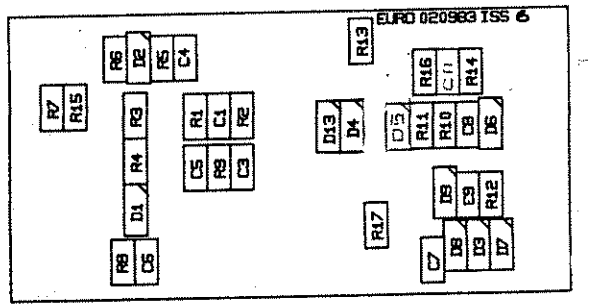


SIDE 2

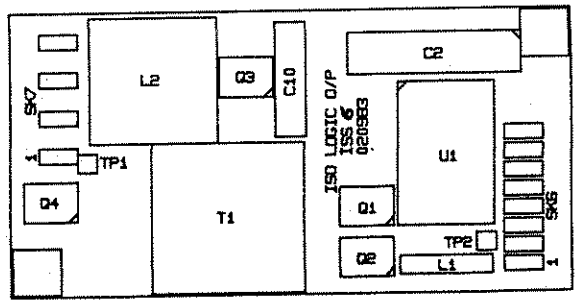


SIDE 1

Figure 8. Logic Output Layout AH020983 Iss 1



SIDE 1



SIDE 2

Figure 9. Logic Output Layout AH020983 Iss 3

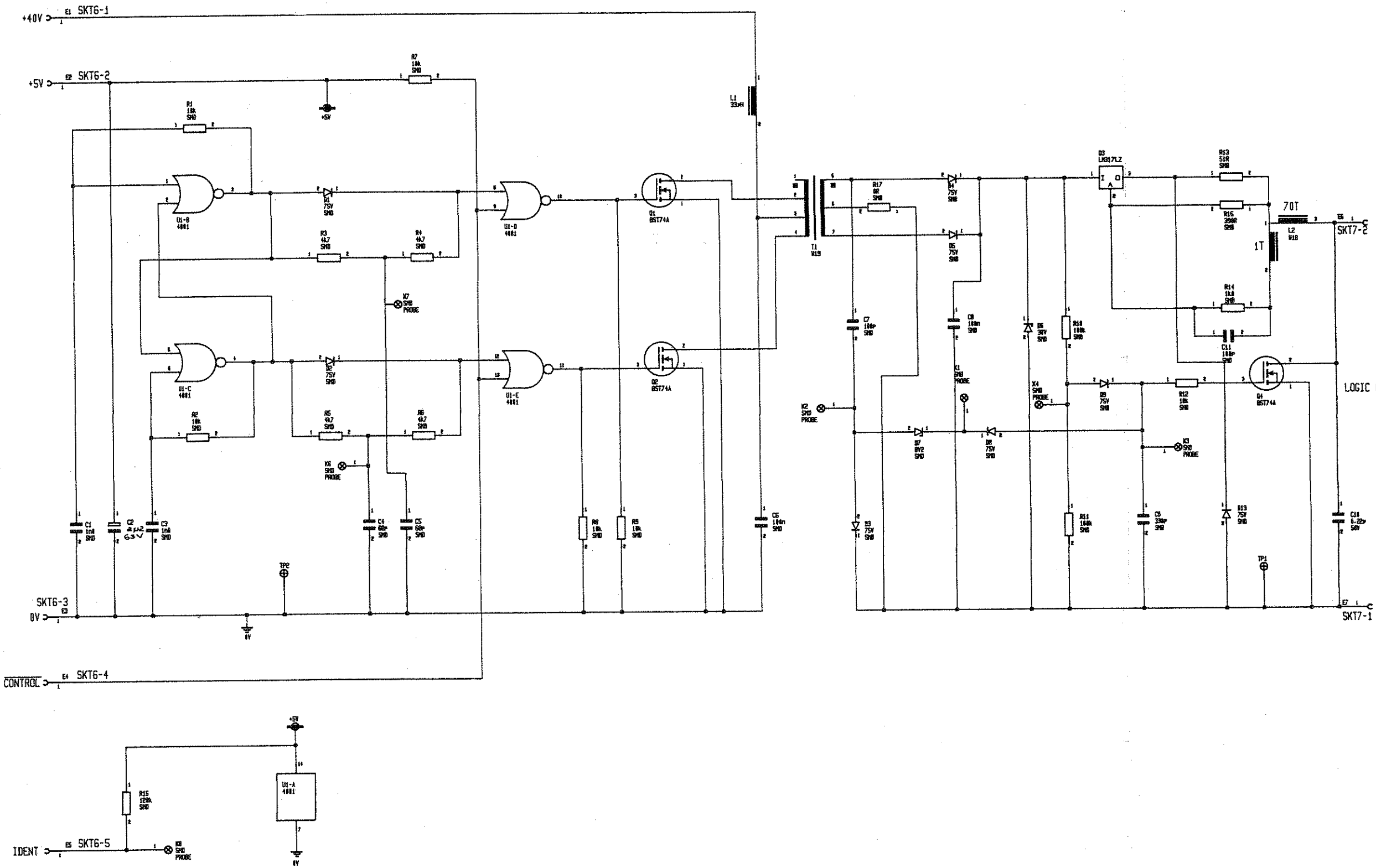
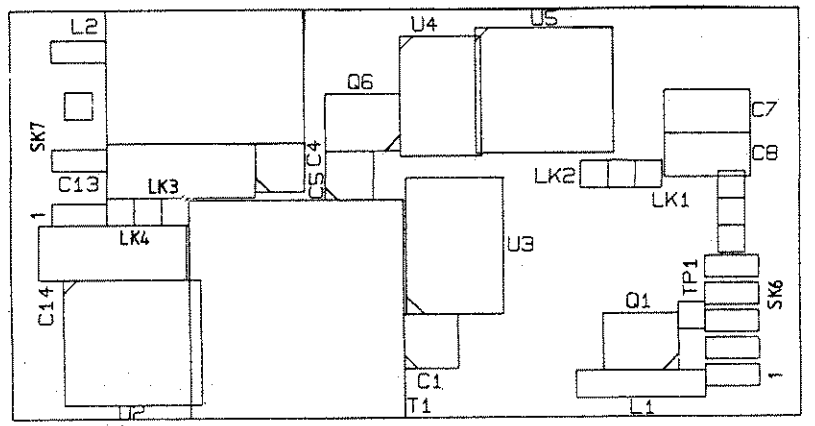


Figure 10 Logic Output Circuit Diagram
AI020983 Iss 4



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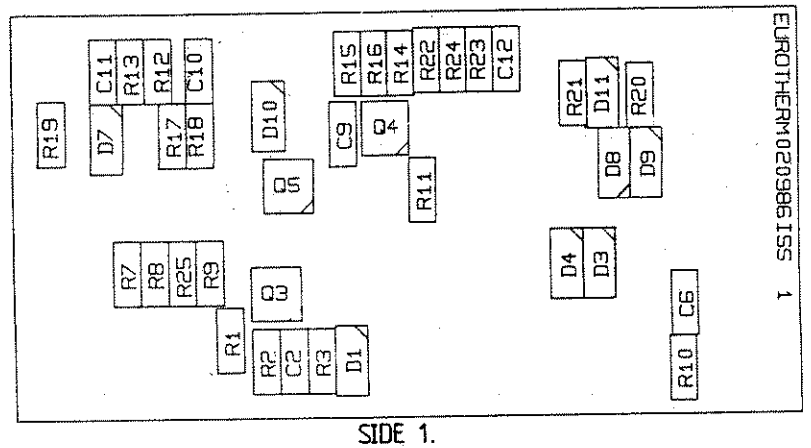


SIDE 1.

Figure 11. DC Retransmission Layout AH020986 Iss 2

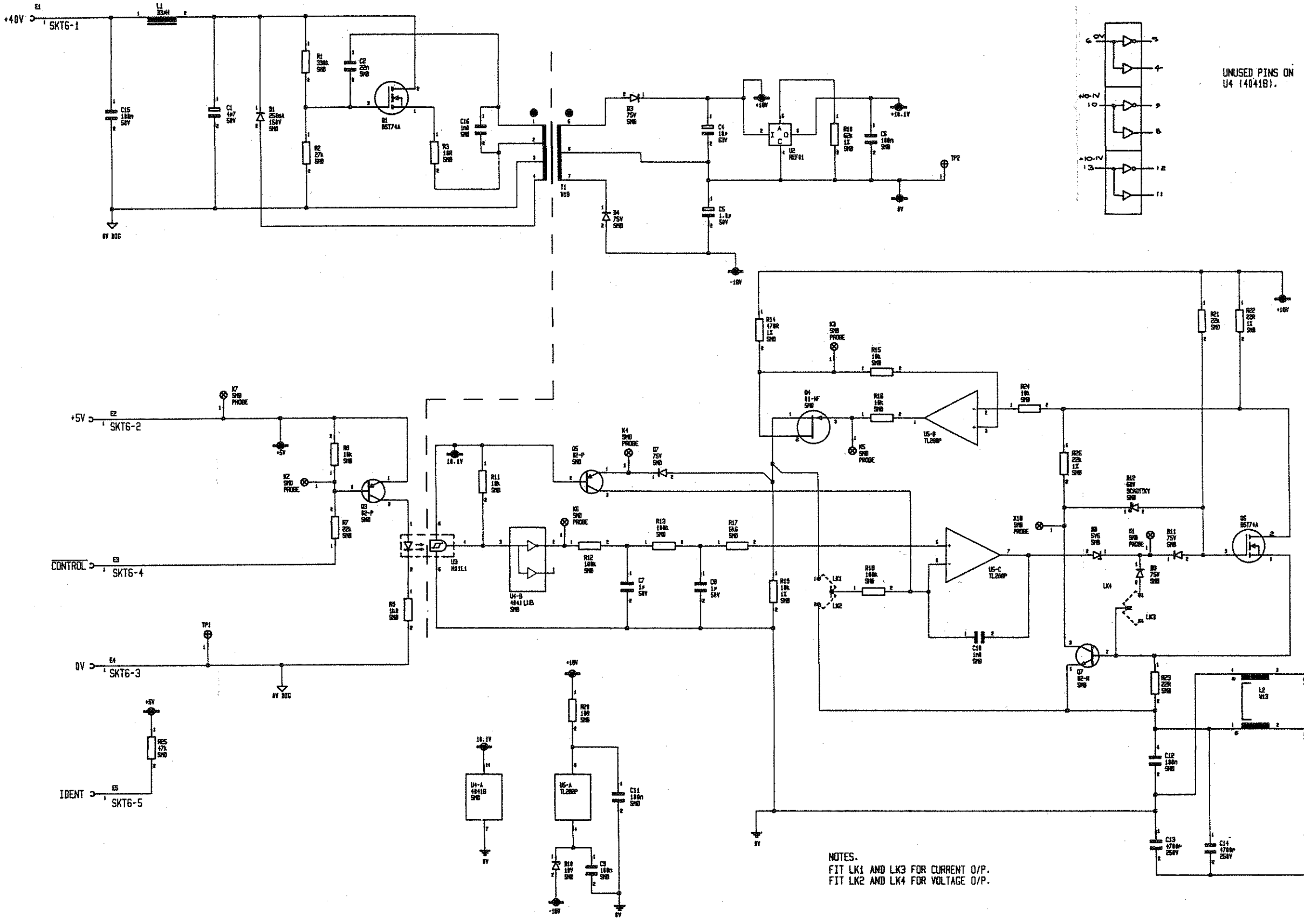
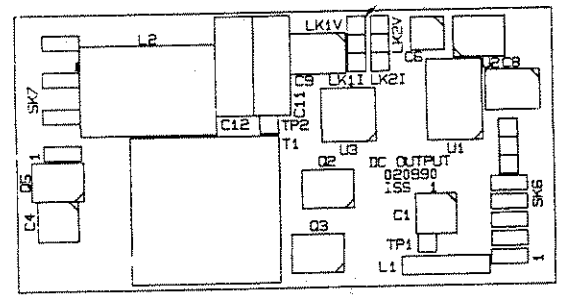
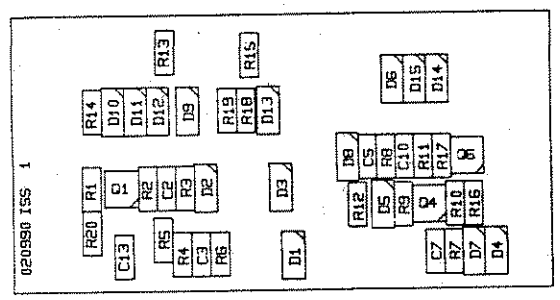


Figure 12 DC Retransmission Circuit Diagram
AI020986 Iss 6



SIDE 2.



SIDE 1.

Figure 13. DC Output Layout AH020990 Iss 1

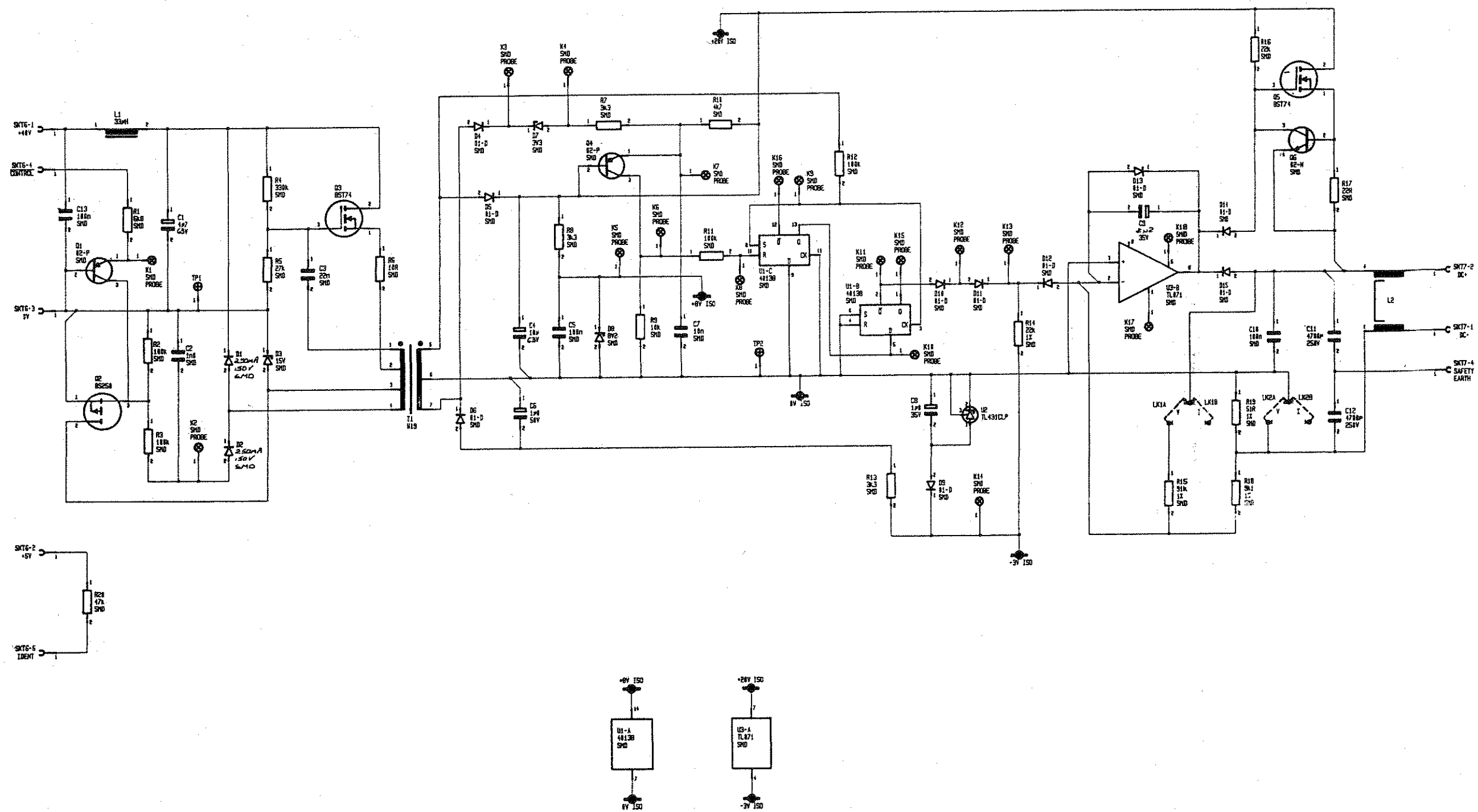
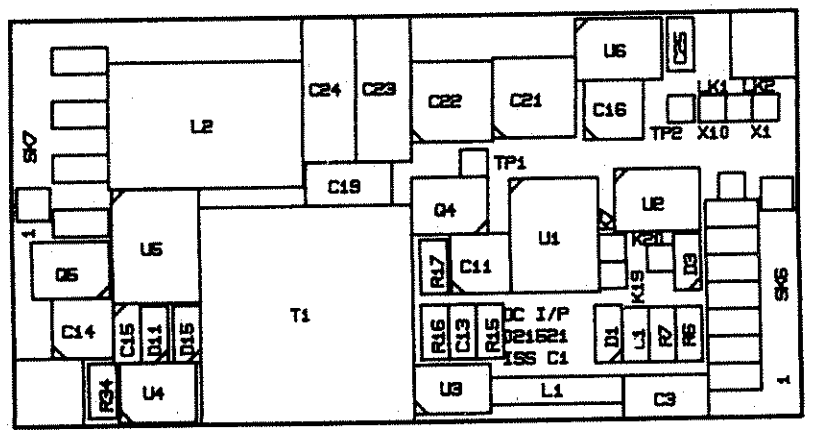


Figure 14 DC Output Circuit Diagram
AI020990 Iss 1



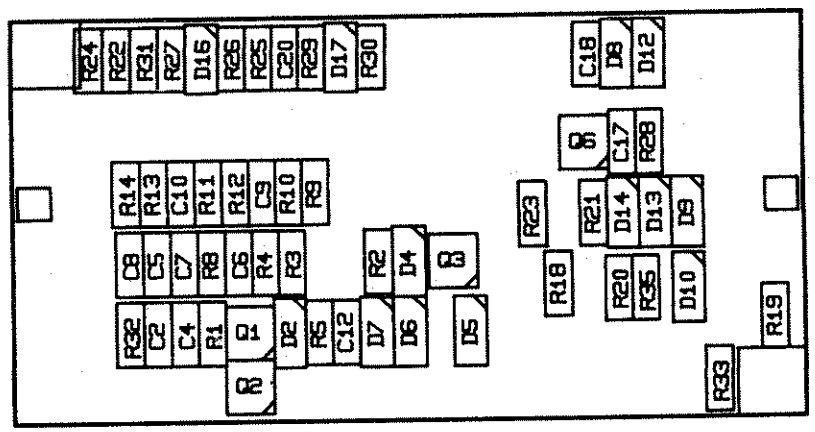


Figure 15. DC Input Layout AH021521U001 Iss 3

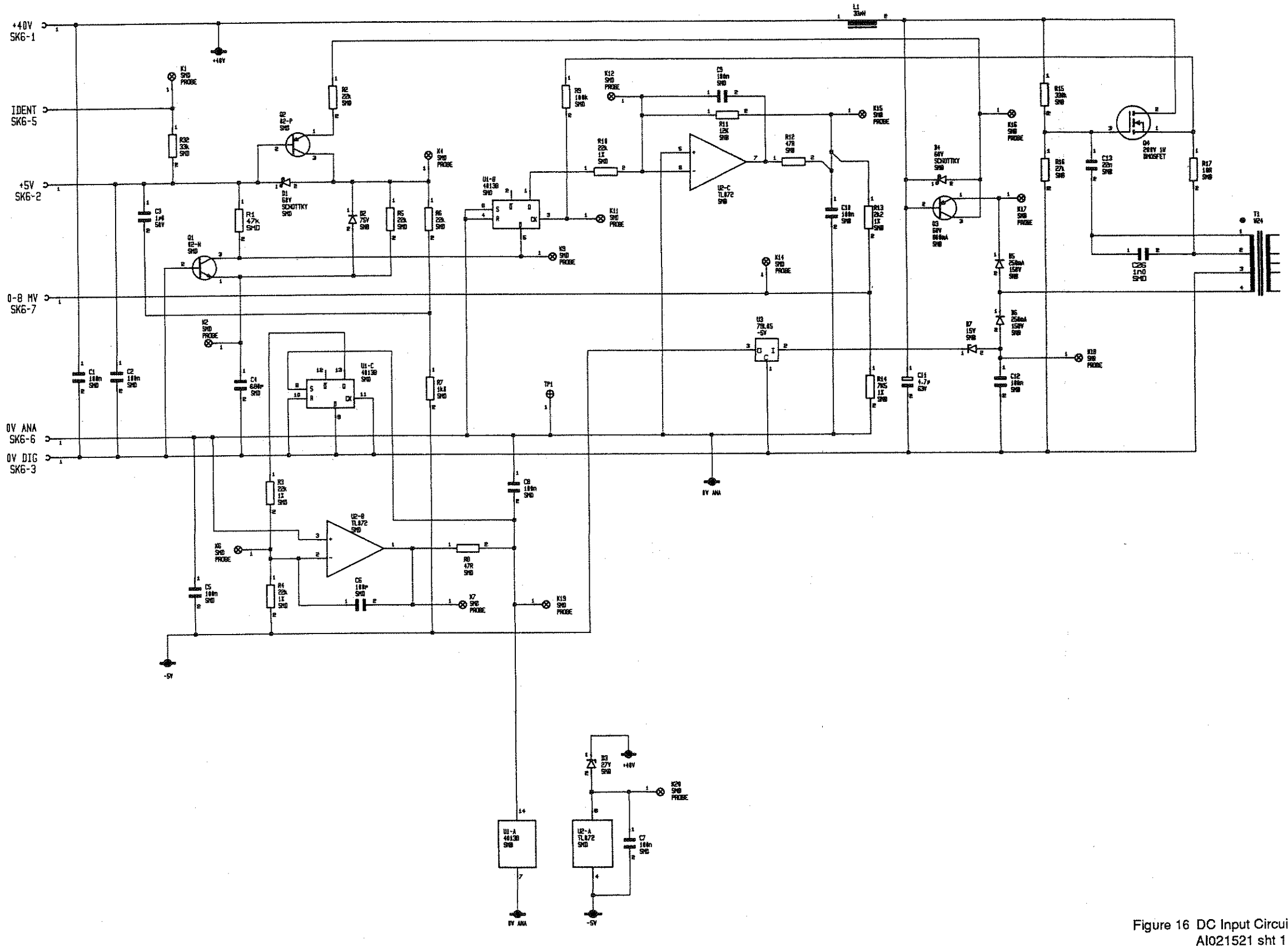
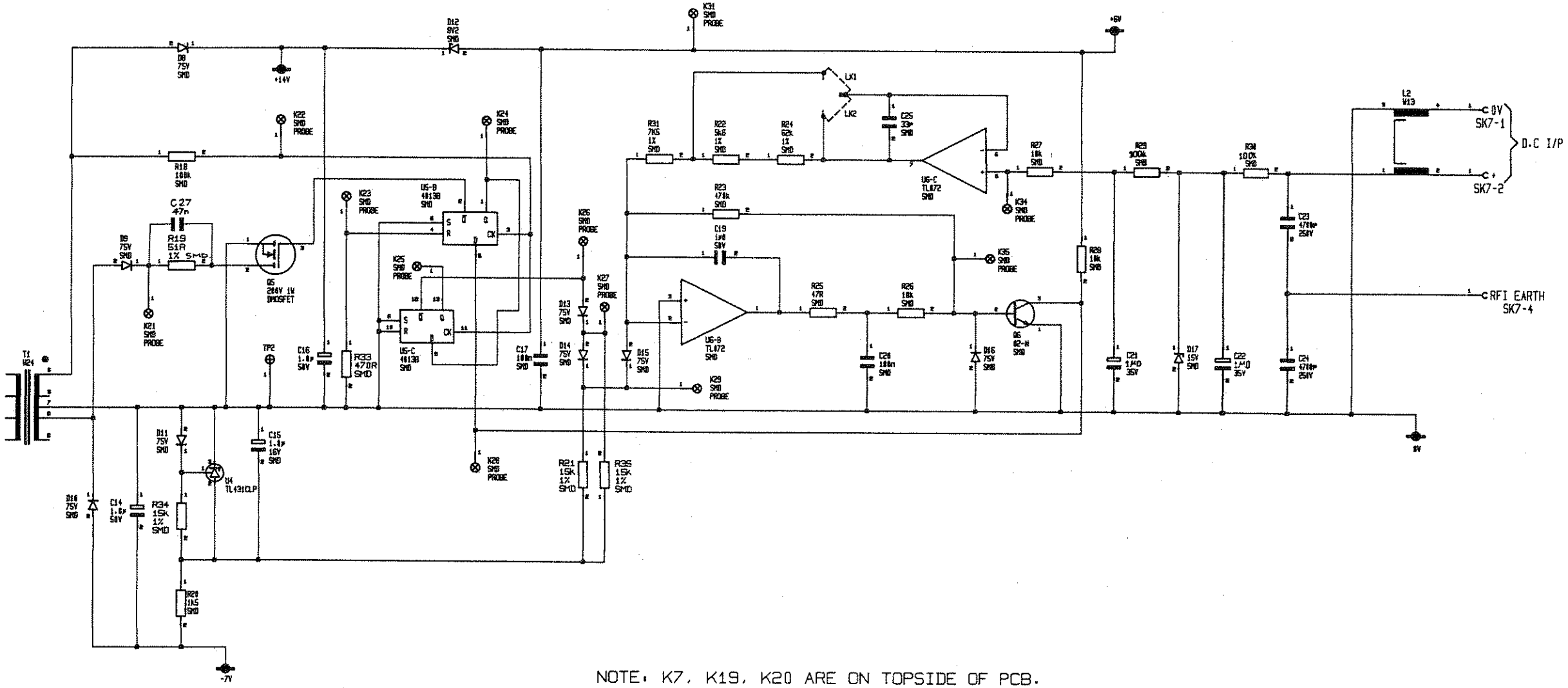


Figure 16 DC Input Circuit Diagram
AI021521 sht 1 Iss 3



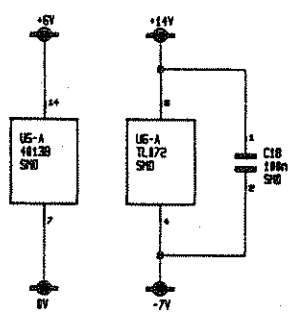
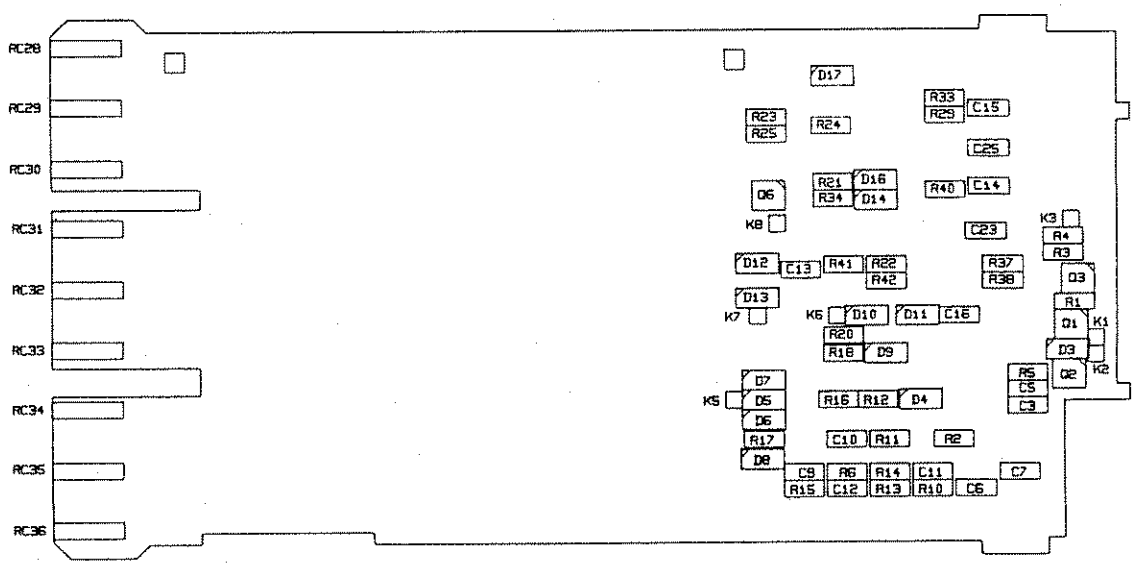


Figure 17 DC Input Circuit Diagram
AI021521U001 sht 2 Iss 3



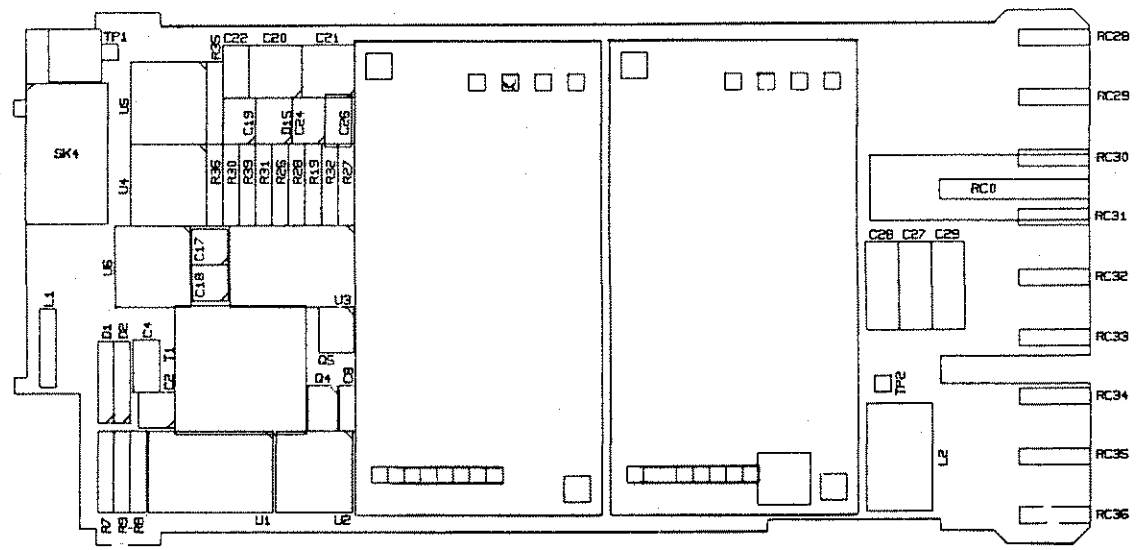


Figure 18. Valve Positioner Layout AH021415 Iss B1

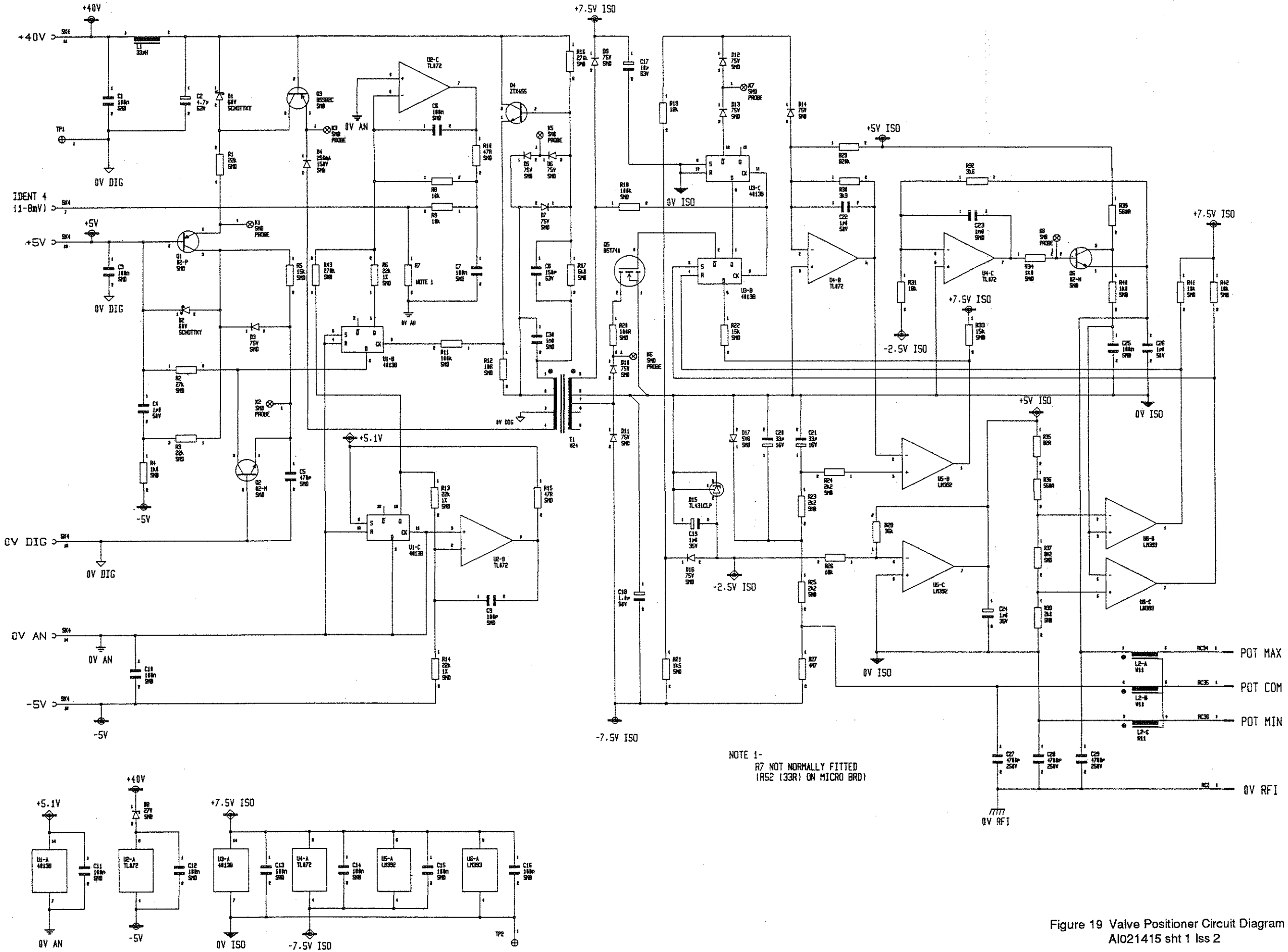


Figure 19 Valve Positioner Circuit Diagram
AI021415 sht 1 Iss 2

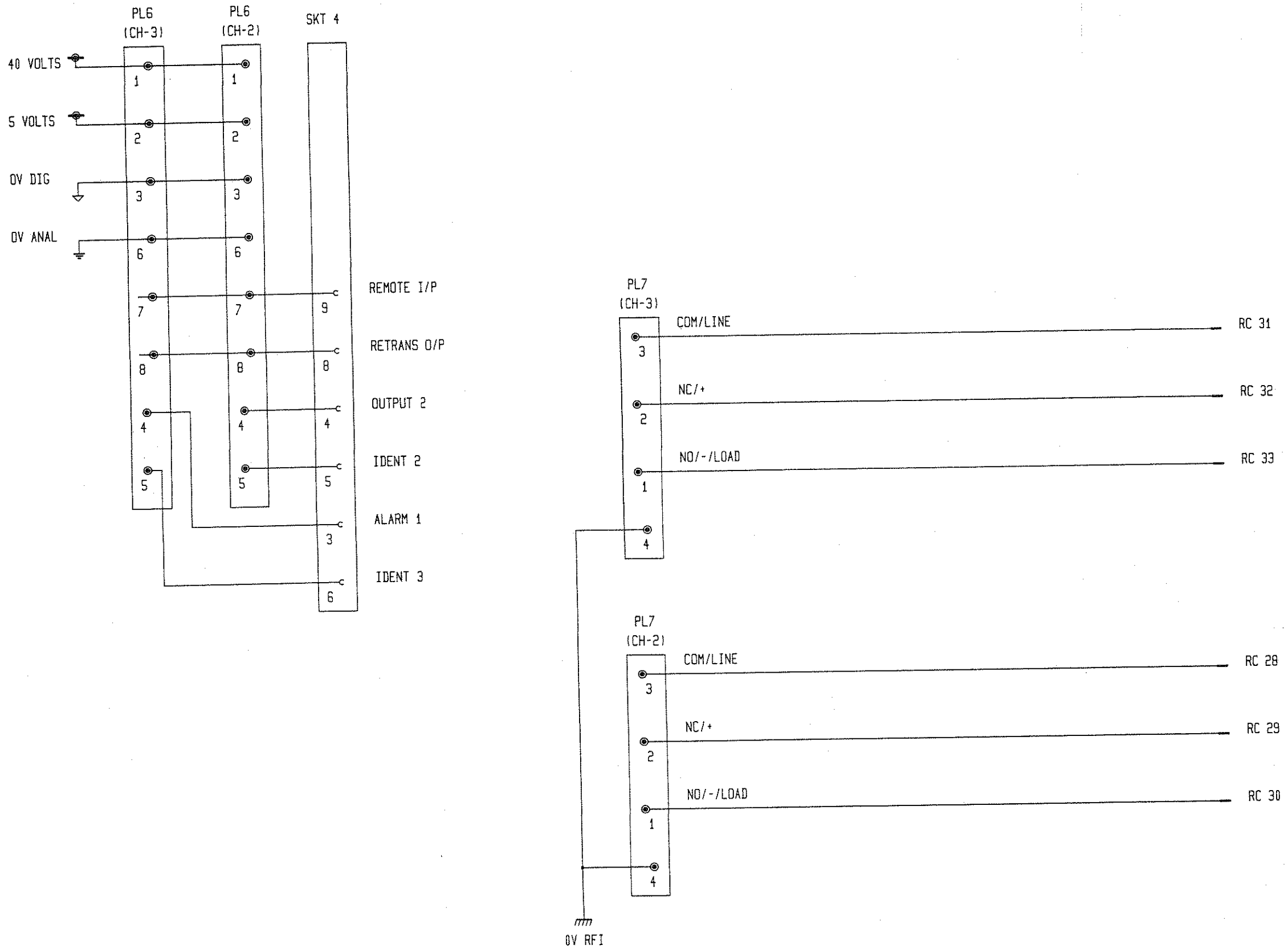


Figure 20 Valve Positioner Circuit Diagram
AI021415 sht 2 Iss 2

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