414/415
3 PHASE STACK

CONTENTS

1. SPECIFICATION

1 i. Electrical Specification

a. Load Currents

414:	25A, 50A and 75A	convection cooled.
	100A and 150A	fan cooled.
415:	175A and 225A	convection cooled.
	330A and 500A	fan cooled.

b. Supply Volts

220V, 240V. +10% -15%
380V, 415V.
440V.
460V, 480V, 500V.
660V.

c. Load Configuration

3-wire delta, 3 and 4-wire star. Link selectable.
6-wire delta optional.

d. Power Ratings

3 or 4-wire - RMS load current x line to line volts x $/\overline{3}$
6-wire - RMS load current x line to line volts x 3

d. Control Signal Input

0-5V, 1-5V, 0-10V.	@ 50K ohms.
0-5mA, 0-10mA.	@ 1K ohms.
0-20mA, 4-20mA.	@ 250 ohms.

Link selectable.

e. Firing Mode

Phase angle. 100mS ramp on/ramp off.
Phase angle. 2S ramp on / ramp off.
Fast cycle. 0.4S on + 0.4S off @ 50%
Fast cycle with soft start.
Slow cycle. 10S on + 10S off @ 50%
Slow cycle with soft start.
Link selectable

f. Feedback Mode

Voltage mean-squared
Current mean-squared
Voltage times currents

g. Control Linearity

Better than +/-1% for mean-squared voltage control.

h. Control Stability

Better than +/-1% for +10%, -15% symmetrical mains variation.

1 i. Electrical Specification

j. Other Facilities

Current Limit	Highest of three line currents. Internal pre-set or external 0-10V signal in cascade with internal pre-set.
Power Demand Limit	Clamp on demand input signal. Internal pre-set or external 0-10V signal in cascade with internal pre-set.
Voltage Current Transfer	Current limit setting varies with control input giving a transfer from current control to voltage control for low cold resistance loads.
Chop Off	Fast quench of thyristor stack due to half cycle overload. Automatic restart with lock out after four shut downs.
Inhibit	+5V to +30V @ 10K ohms. Applied signal will inhibit output. Open circuit to release.
Feedback Monitor	Buffered 0V to +10V @ 5mA. Measured feedback signal. 8.2V = 100% power (nominal supply).
Current Monitor	Buffered 0V to +10V @ 5mA. Phasor sum of three line currents. 10V = full rated current.
Manual Input	Provision for 4K7 or 10K potentiometer. Input impedance = 10K ohms.
User +10V	+10.0V @ 10mA.
Diagnostic Socket	20 way diagnostic connector for use with type 260 diagnostic unit.

1 ii. Environmental Specification

Temperature	0 - 55 deg C convection cooled 0 - 45 deg C fan cooled Derating curves for higher temperatures.
Humidity	93% RH @ 40 deg C.
Altitude	1% derating per 100 meters above sea level.

1 iii. Mechanical Specification

Dimensions and Weight	Height (mm)	Width (mm)	Depth (mm)	Weight (Kg)
Model				
414	420	190	220	14
415	420	500	270	40

Fixings	By 6mm bolts	
Fixing centers	414	90mm x 391mm
	415	180mm x 391mm

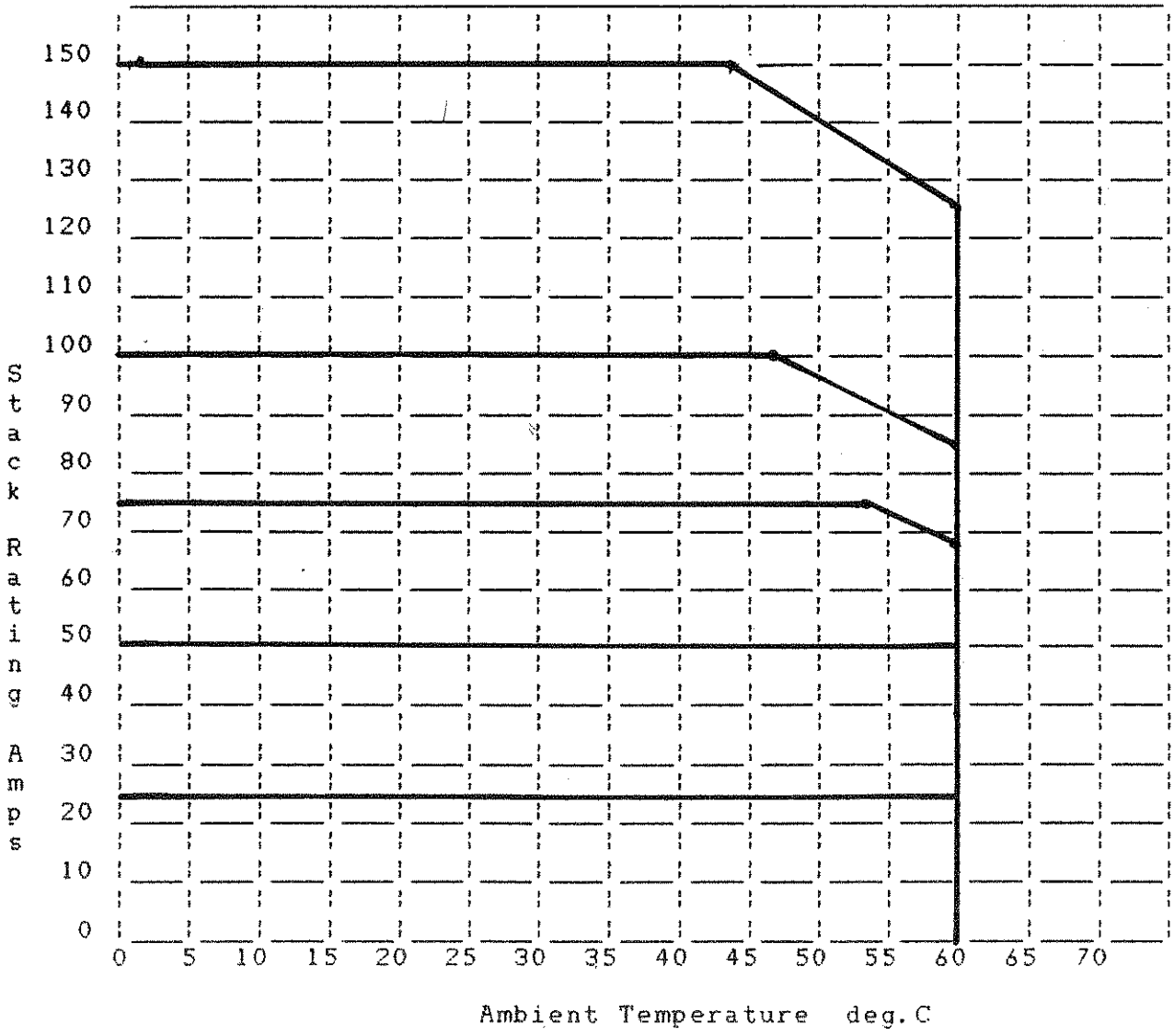
Fixing can also	be made via Din rail.
Din rail	BC048759 in 3 meter lengths.
Captive nut	FZ048752 each. (4off 414, 6off 415).

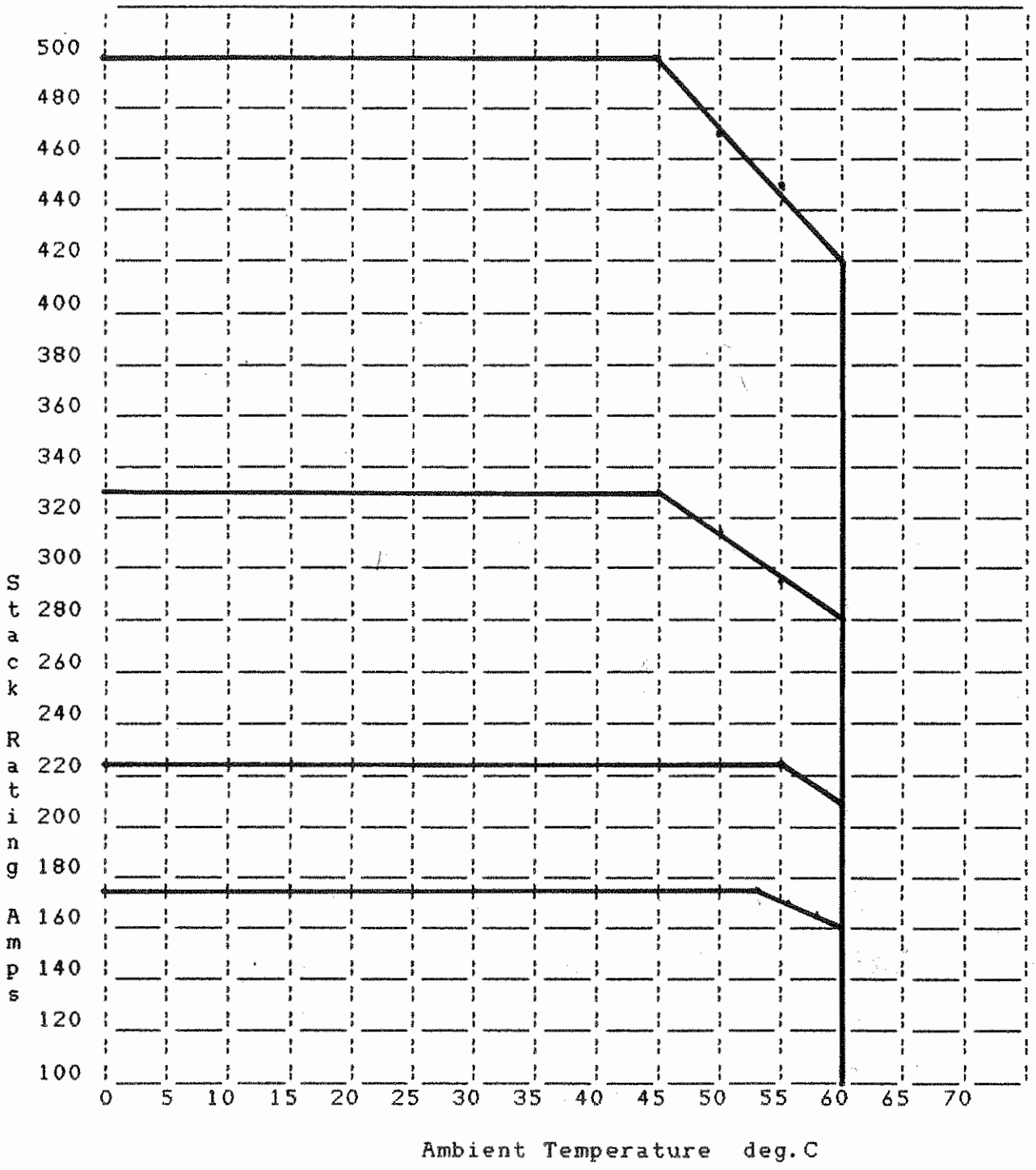
Operating Temperature

The maximum temperature of the air entering the bottom of the thyristor unit shall not exceed 55 deg.C for convection cooled units and 45 deg.C for fan cooled units. The minimum operating temperature in both cases is 0 deg.C.

In some cases it may be possible to exceed the operating temperature. Consult your Eurotherm engineer or refer to derating curves.

eg. A 100 amp thyristor unit is to be used to control a 60kW 3-wire delta load from a 415V +/-7% supply. (Allowing for the worst case condition, i.e. a +7% increase in the supply voltage, the maximum thyristor current would be 89 amps). From the curve an 89% derating of an 100A fan cooled thyristor unit will allow the maximum ambient temperature to rise to 56 deg.C.




500
480
460
440
420
400
380
360
340
320
300
280
260
240
220
200
180
160
140
120
100
Stack Rating Amps
0
5
10
15
20
25
30
35
40
45
50
55
60
65
70
Ambient Temperature deg.C

2 i. Wiring - 414

a. Power Terminals

Power cables are connected to the bottom of the unit with an 8mm nut and bolt. The three line inputs are at the front under the main fuses. The three load outputs are at the left hand side and are in the same order, when viewing them left to right, as the line input terminals. The Earth terminal is at the rear behind the load terminals and, for convenience, should be connected first.

b. Signal Terminals

The control signal connections are made to the top of the unit via a 12-way terminal block located on the top edge of the front pcb. Looking at the front the terminals are numbered 1 - 12 from left to right.

The function of the terminals are as follows:-

1. 0V. signal.
2. Control signal input.
3. Manual input.
4. 0V. limit signal.
5. 10V. supply.
6. External limit input.
7. Chop off reset.
8. Current monitor signal.
9. Feedback monitor signal.
10. 0V. supply.
11. Inhibit.
12. Temperature trip indication.

2 ii. Wiring - 415

a. Power Terminals

Power cables are connected to the unit with a 10mm nut and bolt. The three line inputs are at the top front of the unit above the main fuses. The three load outputs are at the bottom front of the unit. The load terminals are in the same order, left to right as the line input terminals.

b. Signal Terminals

The control signal connections are made to the top of the unit via a 12-way terminal block located on the top edge of the front pcb. Looking at the front the terminals are numbered 1 - 12 from left to right.

The function of the terminals are as follows:-

1. 0V. signal.
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7. Chop off reset.
8. Current monitor signal.
9. Feedback monitor signal.
10. 0V. supply.
11. Inhibit.
12. Temperature trip indication.

3. OPERATION

3 i. User adjustments

There are three pots available to the customer. P1 is at the top P2 in the middle and P3 is the bottom pot.

a. P1 Power Scaling

P1 power scaling provides a +/- 20% power adjustment to take up a 10% variation in line volts or full scale load current. Power increases as pot is turned clockwise.

b. P2 Soft Start adjust

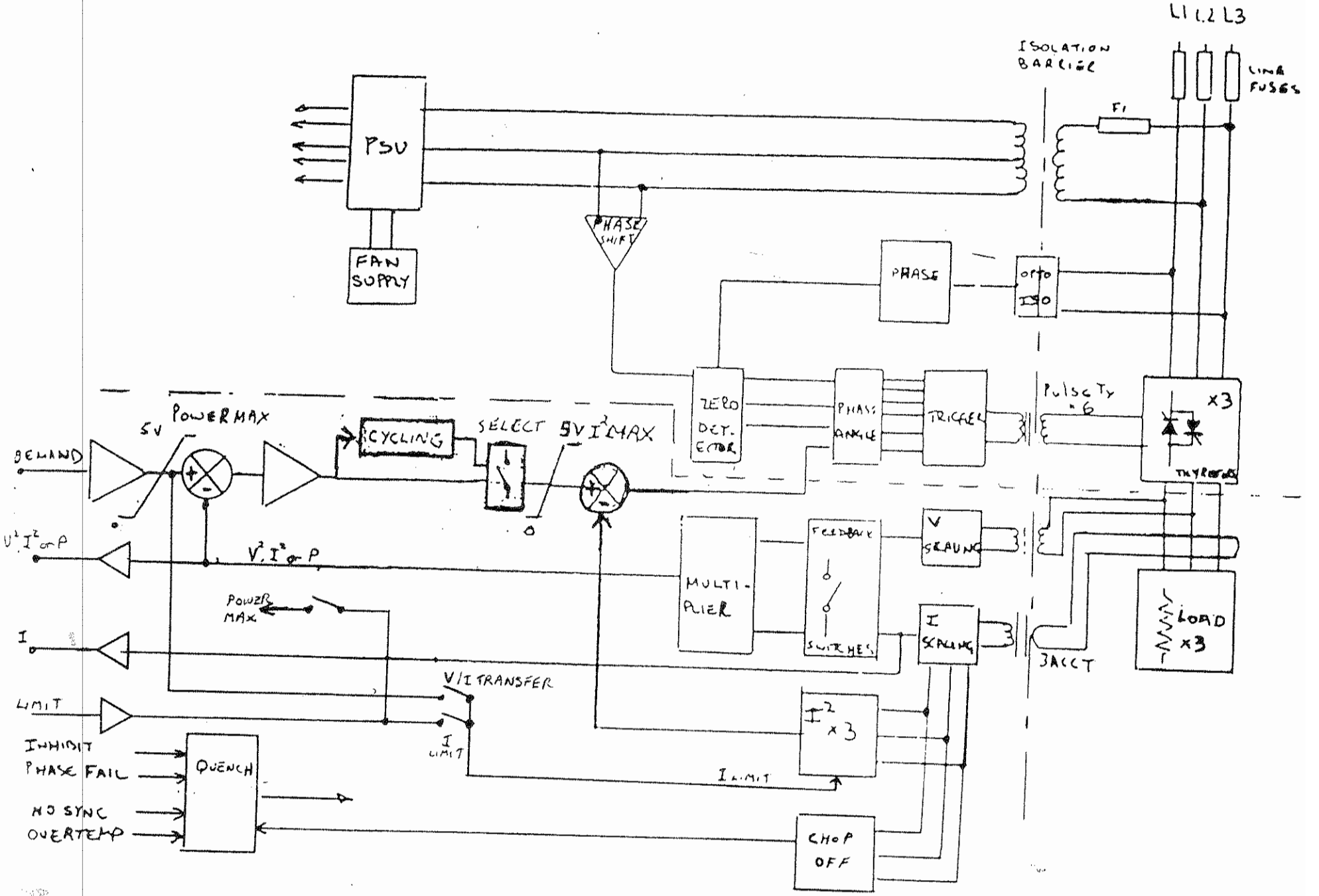
P2 is only operative in cycling mode and varies the number of cycles it takes to phase up to and down from full conduction. The adjustment is between 3 and 12 cycles. Max delay is with P2 fully clockwise.

c. P3 Limit setting

P3 adjusts the limit threshold setting with link switch 9 set to internal or external. Power increases (i.e minimum limit) with P3 turned clockwise.

Internal preset RV5 located on the control pcb is for current scaling. This is set in the factory at the full current rating of the unit.

414/S BLOCK DIAGRAM



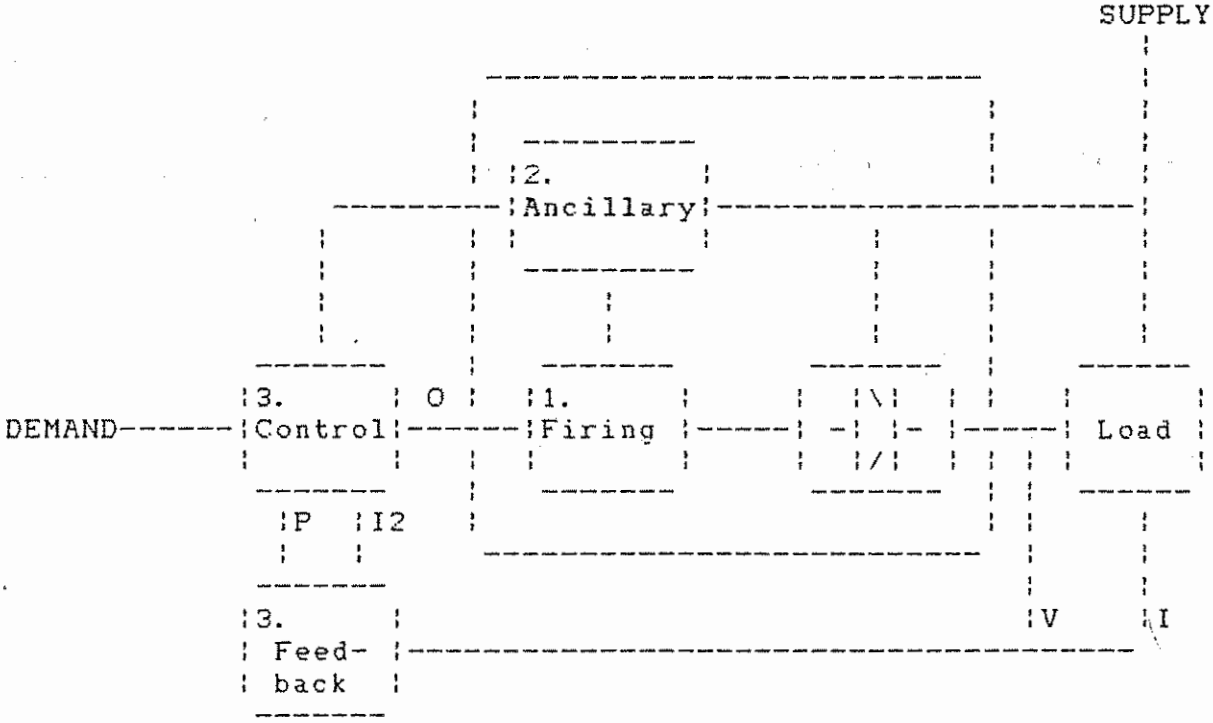
4. THREE PHASE STACK CIRCUIT FUNCTIONALITY

4 i. Preamble

The functional requirements of the stack were placed into three groups. The first grouping was called the firing circuit and includes all functional blocks related to the synchronisation and triggering of the main devices.

The second grouping was called the auxillary circuits and includes psu, protection circuit and peripheral circuits not included in groups one or three. The first two groups on their own could form the basis of a simple, open loop stack.

The third grouping was called the control circuit. This grouping includes signal conditioning circuitry for the current limit and power loops.



THREE PHASE STACK CIRCUIT FUNCTIONALITY

4 ii. Firing Circuits

a. Zero Crossing

The correct determination of the zero crossing position is fundamental to the proper working of the unit. Errors of synchronisation can have catastrophic effects on transformer and low cold resistance loads. To make this unit resilient to line transients a phase lock loop technique is used to synthesize the six zero crossing points.

The synchronising signal is taking from the mains transformer T11 and is applied to CN2-19. It then passes through a 90 degree filter formed by R112 and C26. This ensures a negligible phase shift for a 50Hz to 60Hz change in supply frequency while giving a high degree of noise immunity. As the amplitude of this signal is greatly reduced by the filter there must be no dc shift between it and its reference zero. The 0v from the centre tap of the mains transformer moves with respect to its ends because of the unbalanced loading on the transformer, so an artificial reference point is generated by R58 and R59.

This signal is presented to IC5.2 which is arranged as a hysteretic switch to give a square wave signal at IC5.1. The 90 degree filter is not perfect so an additional phase shift is provided by R117 and C30. The signal swings between +15V and -15V so R118 is included to convert it to +15V and 0V required for IC9.1.

This squared and delayed signal synchronised to the line supply can be seen at test point 6 (TP6) and is input to the phase lock loop (PLL) at IC10.14. This signal enters a phase comparator which adjusts its output, IC10.13, until the feedback signal on IC10.3 is in phase with the input. The output on IC10.13 is in the form of pulses. These are smoothed by R121, C34 and R122. The smoothed signal is fed back to IC10.9 which is the input to the voltage controlled oscillator (VCO) section of the PLL. The oscillator output is at IC10.4 and the output signal is a square wave which has a frequency 96 times the supply frequency.

This signal enters IC12.9 which is the input to a 4-bit counter. The output of this counter is IC12.14 and provides a 6f clock, a signal whose frequency is six times the supply frequency. The edges of this clock provide the 60 degree and 30 degree steps required for positioning the various zero crossing points. This 6f clock is used to drive a shift register IC12 connected as a ring counter. The outputs of the register are on pins 1, 15 and 14 and they produce the following sequence:

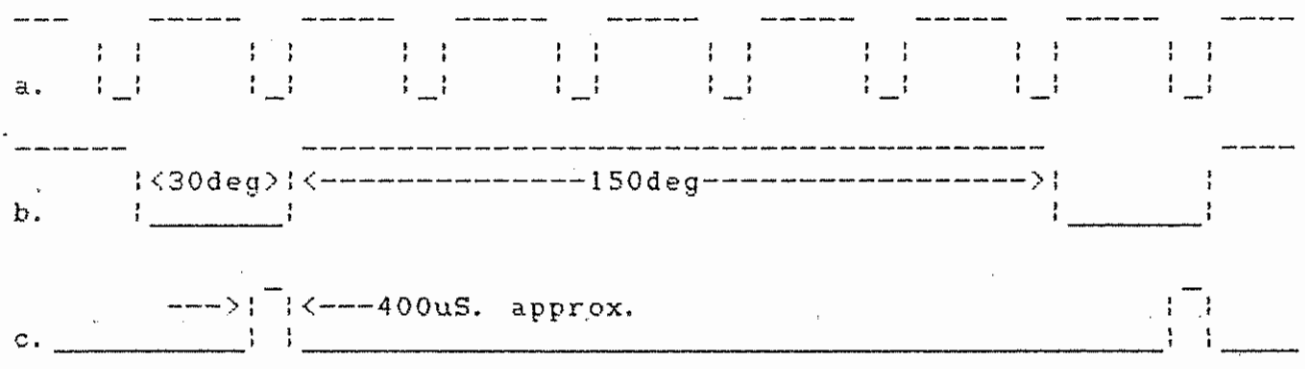
clock pulse	output 1 2 3
1	0 0 0
2	1 0 0
3	1 1 0
4	1 1 1
5	0 1 1
6	0 0 1
repeat pattern	

A 3-bit binary pattern can have eight combinations, there are six in the above table which leaves two illegal combinations, 010 and 101, which must be guarded against. This is done by IC16 and half of IC14. If either of these patterns appear, usually at switch on, then the output at IC16.10 will reset the register IC15.5

If we invert the output from IC15.15 we will then have three square waves displaced by 120 degrees. These three outputs then each go to a D type flip-flop, IC17.9, IC18.5 and IC18.9. The 6f clock is inverted at IC14.10 and appears on testpoint 8 (TP8). As both the shift register IC15, and the flip-flops are positive edge triggered, then because of the inversion, the flip-flops will be clocked 30 degrees after the outputs of the shift register have changed. The delayed outputs will appear on IC17.13, IC18.1 and IC18.13 with an inverted signal on IC17.12, IC18.2 and IC18.12. These signal pairs provide the gating for the positive and negative half cycles for the Red (L1), Yellow (L2) and Blue (L3) phases respectively.

This 30 degree delay is used to give the necessary phase shift on the feedback signal with switches SW10 and SW11. This is required because of the shift in zero crossing points between line to line load connections and line to neutral load connections. The route of the feedback signal will also depend on the phase rotation which will affect the gating signals on IC13.2 and IC13.6.

The data input signals to the flip-flops and their respective delayed outputs are exclusive-nor'd to produce a 30 degree window at outputs IC19.3, IC19.4 and IC19.10. These windows gate a stream of pulses produced from IC13.10. The gated outputs on IC20.3, IC20.4 and IC20.10 are the three zero- crossing pulses, which also appear on TP10, TP11 and TP12. These zero-crossing pulses should be positioned just before the respective mains zero-crossing to ensure there is no sudden step in power from zero.



Waveforms at a). IC20.1, b). IC20.2 and c). IC20.3

Load switches 10 and 11 are used to select the required load configuration. The following table indicates the various switch configurations.

LOAD	SW10	SW11
3 Wire	1	1
4 Wire	2	2

6 Wire loads have the same settings for SW10 and SW11 as 3 Wire, but there is a link change for the voltage feed-back on the High Voltage board.

In the table: 1 = change over link position nearest right hand side of board.
2 = change over link position nearest left hand side of board.

Board to be viewed as per configuration diagram.

4 ii. Firing Circuits

b. Phase Rotation

There are two ways in which the phases can rotate L1,L2,L3 or L3,L2,L1 and the sequence in which the thyristors are fired have to be altered between the two cases. Phase rotation is determined by the phase comparison of two signals. The first is from the synchronising signal used to develope the zero crossing pulses. This signal is picked off from IC9.2 and is used to clock a D type flip-flop at IC17.3. The other signal comes from opto-coupler U2 on the high voltage board this is squared up by Q5 and passed to the control board via CN2.17. This signal will also be on TP9.

The rotation signal will appear at the flip-flop data input at IC17.5 and is clocked through by the signal on IC17.3. Depending on the phase relationship of these two signals either a '0' or a '1' will be appear at IC17.1 This point is available for a type 260 diagnostic unit at diagnostic point 14 where 0V indicates forward rotation and 15V indicates reverse rotation.

4 ii. Firing Circuits

c. Frequency Compensation

The output on IC10.10 is a buffered version of the signal controlling the voltage controlled oscillator in the phase locked loop. As the VCO has to adjust its frequency to track the supply frequency and as there is a linear relationship between this frequency and the control input, then this output on IC10.10 can be used to compensate for changes in supply frequency.

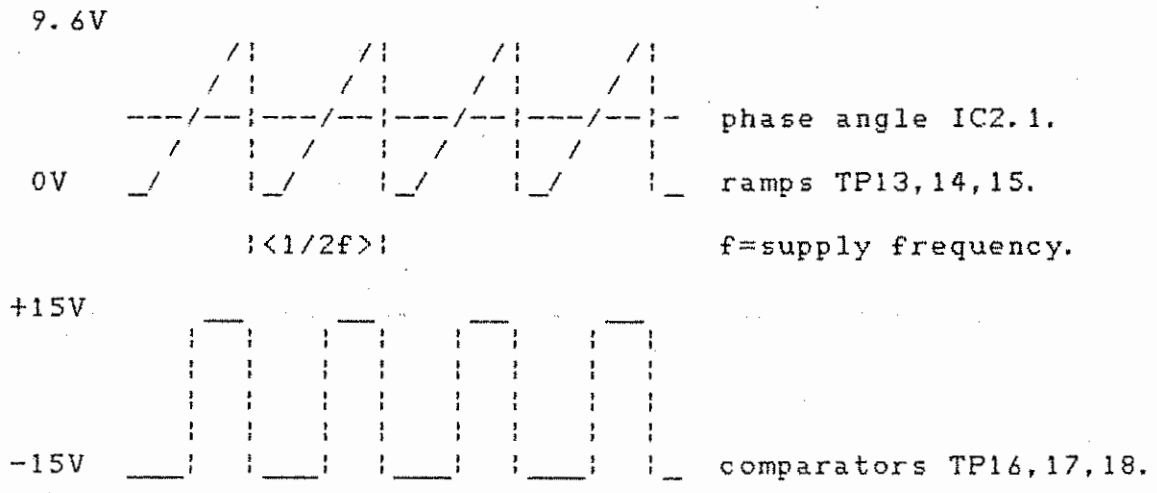
This compensation signal is level shifted to give at IC21.1 a voltage which is -1.0V at a frequency of 50Hz and -1.2V at 60Hz and it is used as the reference signal for the generation of the three timing ramps from which the phase angle is derived. The voltage level is available at diagnostic point 16.

4 ii. Firing Circuits

d. Phase Angle

The phase angle is determined by comparing the phase angle signal with three timing ramps. The three timing ramps are generated by IC21.7, .8 and .14 and can be seen at test points TP13, TP14 and TP15. The time constant of these ramps is 1mS. which is set by components R163/C48, R164/C51 and R165/C54. This will give a ramp of 0V to about 9.6V. The ramp would have reached 10V in a half mains cycle if it was not for the 400uS. zero crossing pulse turning on the gates of IC32.13, .6 and .12, which shorts the timing capacitor and so drives the ramp back to zero.

This ramp is compared with the phase angle signal such that when the ramp exceeds the phase angle signal the output of the comparators go high (+15V) producing a command to fire signal at TP16, TP17 and TP18. These three command signals determine the triggering of the thyristors.



Waveforms generated by the phase angle demand signal.

4 ii. Firing Circuits

e. Triggering

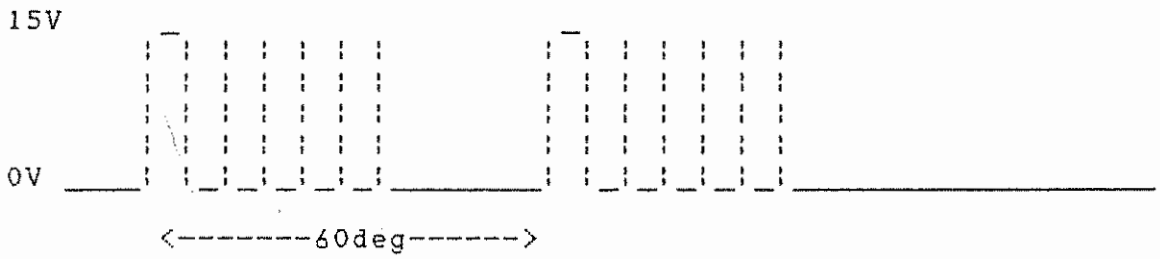
In a giving mains cycle in a three phase system there are six trigger points one for each thyristor. These trigger points are the plus and minus halves of each phase and can be seen at the outputs of IC23.3, .4, .10, .11 and IC24.3 and .4. The trigger point is when the output goes low.

In a three wire system although there are still six trigger points there are two for each thyristor. When a thyristor is fired the current flowing through it must return to the suply via another thyristor. Therefore to ensure that this second thyristor is in conduction it receives a firing pulse at the same time. This cross-coupling of the trigger pulses is performed by IC25.3, .4, .10 and .11 and IC26.3 and .4.

The trigger pulses to the thyristors are in the form of a pulse train. A common oscillator is employed, the output of which is at IC6.1. This is a square wave output with a nominal frequency of 250 kHz and can be seen at TP19. This signal is the clock input of a four-bit counter IC12.1. The last two stages of this counter are output at IC12.5 and .6 and these are fed to a dual input Nor, the output at IC11.10 will give a rectangular wave shape with a 1:3 mark space ratio.

Every time a command to fire signal is giving, say from IC23.3, then via the monostable formed by R135, C38, D21 and R136 there will be produced a short pulse typically 70uS. which will reset the counter. This occurs for each command to fire signal and the six reset signals are wire-or'd together and appear at IC9.8. This train of reset pulses can be seen at diagnostic point 17. These pulses should be 3.3mS (50Hz) apart or 2.8mS (60Hz) but will not be present if no output is demanded.

These reset pulses synchronise the the firing pulse train to the command to fire signals but more immportantly ensure that a substantial pulse appears at the beginning of each trigger point. These reset pulses are effectively mixed with the firing pulse train and can be seen at TP20 as a continuous stream of pulses unless inhibited by the disable signal at IC26.8.



Thyristor firing pulse train at CN2.6 to CN2.11.

This continuous stream of pulses is gated at IC30 and IC31 to give a train of pulses no longer than 120 degrees of the of the main cycle. As the demand signal increases two pulse trains 60 degrees apart will appear at the outputs of these two IC's. These two trains will have a fat first pulse followed by a train of thinner pulses. When these two trains are 60 degrees wide the second train will have merged with the first to produce a pulse train 120 degrees wide. The leading edge will continue to advance but the trailing edge is now truncated by the following phase signal. The following phase will be dependent on the phase rotation. There are two rotation sequences possible. These are:

Forward	Reverse
R+Y-	B+Y-
R+B-	B+R-
Y+B-	Y+R-
Y+R-	Y+B-
B+R-	R+B-
B+Y-	R+Y-

where R is Line1, Y is Line2 and B is Line3.

IC27 and IC28 will gate through the correct truncation signal according to the rotation signal at IC17.1.

THREE PHASE STACK CIRCUIT FUNCTIONALITY

4 iii. Ancillary Circuits

a. Power Supplies

The control circuit supply is derived from T11 which is a connected between the 2nd and 3rd input lines. The tap input is 403V for use on 380V or 415V supplies and the end input is 486V for use on 440V to 500V supplies. The low voltage mains transformer has an end input of 230V for 220V and 240V supplies, its tap voltage is 105V.

The transformer secondary is centre tapped to give 20-0-20 supplies. These are full wave rectified by diodes D26 to D29 and then smoothed to give a nominal +26V and -26V dc supplies for the fan, pulse transformers and +15V and -15V regulated supplies.

The +15V and -15V are generated by U3 and U4 which are three terminal regulators. C20 and C21 are required by the regulators for stability.

On the control card a 10V reference is generated at IC1.1. It uses a 6V5 50 ppm zener D1 as its reference source and is adjusted by RV1. This 10Vref is buffered at IC1.7 and output on terminal 5 of the 12-way small signal terminal to give a user 10V signal. The current drive capability of this signal is 10mA minimum.

4 iii. Ancillary Circuits

b. Device Protection

All semiconductors have limited capabilities and thyristors are no exception. Reliable and satisfactory use of thyristors depends on ensuring that at all times the circuit conditions imposed on them are within their capabilities. To achieve this. the thyristor has to be surrounded by components chosen to protect it against the extreme conditions.

Four modes of protection exist on these units. Firstly the devices are protected against short circuit currents by the in-line fuses, where the I2t of the fuse must be less than that for the device. Secondly the devices must be protected from excessive rate of change of volts, dV/dt, across them. This is accomplished by snubber components C5 R22, C10 R34, C18 R51 working in conjunction with the natural line inductance.

The third mode of protection is to prevent the voltage impressed across the devices from exceeding their maximum rating. The snubber will help towards this end but the main protection is achieved by the inclusion of MOV's R25, R35 and R52. These will guard against transients from the line, due to other equipment being switched, by passing them through to the load. Although transients from the load will be passed through and absorb in the line, under fault conditions in some applications, these transients can exceed the energy rating of the MOV.

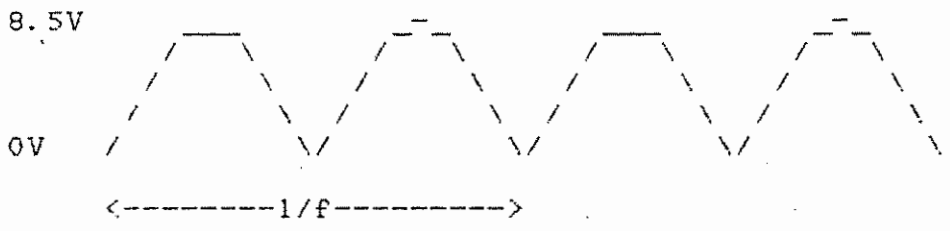
The fourth mode of protection is by means of a thermal trip mounted on the heatsink. This is to guard against thermal overload caused by the restriction of cool air over the heatsink fins. This is fitted as standard on forced air cooled units to guard against fan failure. but can be fitted to any unit. In the case of the 415 there is a thermal trip on each heatsink.

The three trips are wired in series so that the switching of any one will cause the stack to shut down. This shut down is not latched so that once the heatsink has cooled the stack will run up again. The switch(es) are connected to the +15V line via R61 on the High Voltage board. The other end of the switch(es) are connected to R25 on the Control board, this junction also appears at terminal 12 on the small signal terminal block. The switch is normally closed. If the switch opens, this will cause IC24.10 to go high which inhibits the stack and turns on the red LED.

4 iii. Ancillary Circuits

c. Line Failure

Line failure is detected when there is insufficient energy in the supplies to correctly fire the thyristors. This energy is taken from the secondary of the mains transformer, T11, off of smoothing capacitor C12. The secondary supply volts is fed via pin 19 of the 31-way pcb connector to the back to back diode pair D4 and D5. This produces a full wave rectified signal at IC5.7 which can be seen on diagnostic point 6.



Waveform at diagnostic point 6.

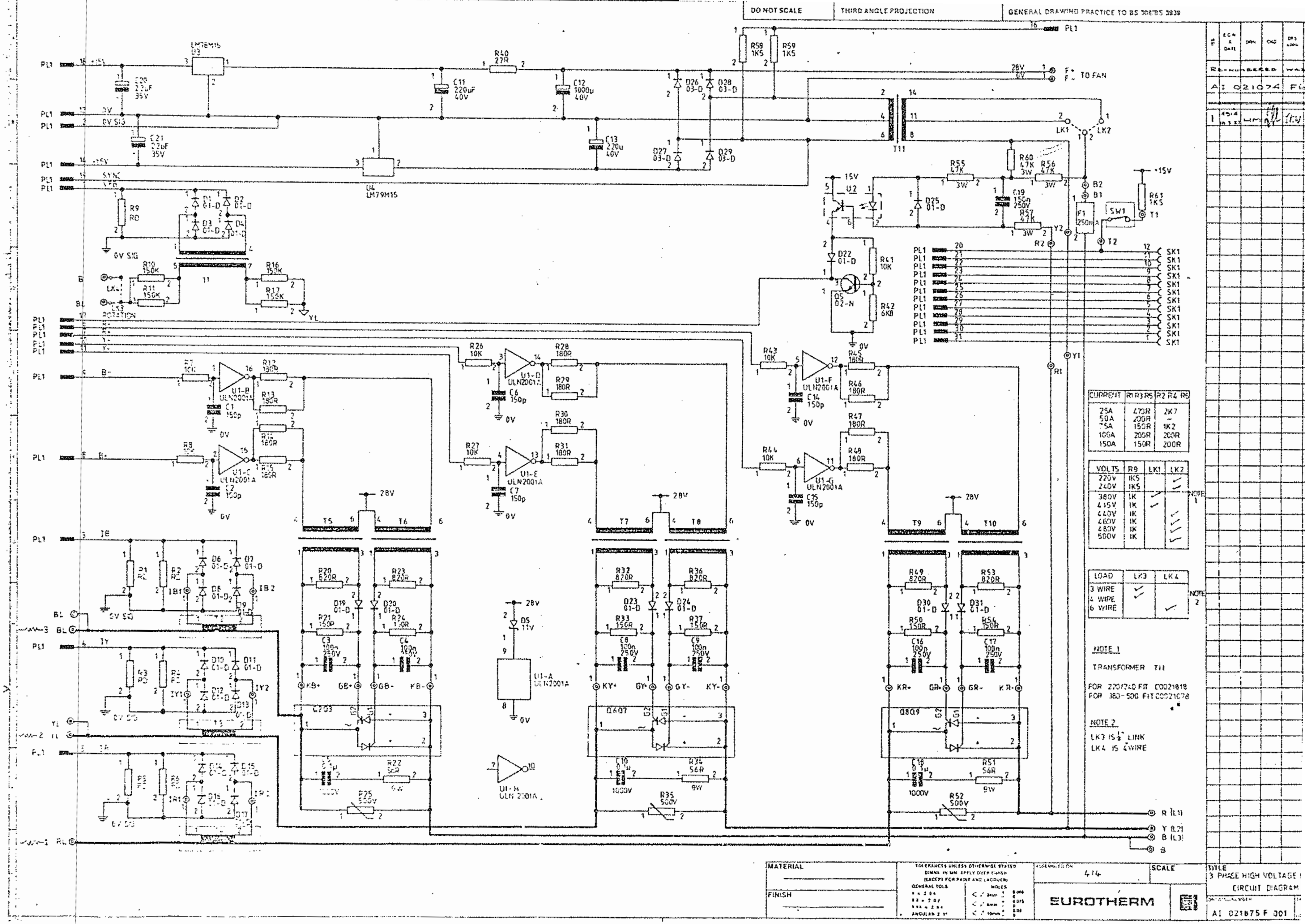
This signal will continually charge capacitor C11 via D6 every half mains cycle. The voltage on C11 is compared at IC6.6 and if its level falls too low then the output of the comparator IC6.7 will go high. This signal is inverted and mixed with the synch enable and when both signals are high IC26.11 goes low and the green LED will come on. At the same time the square wave on the Rotation signal is monitored. If this signal goes high then TR8 will cease to discharge C58. The Fail signal will go low pulling IC6.6 down and so causing the comparator to trip.

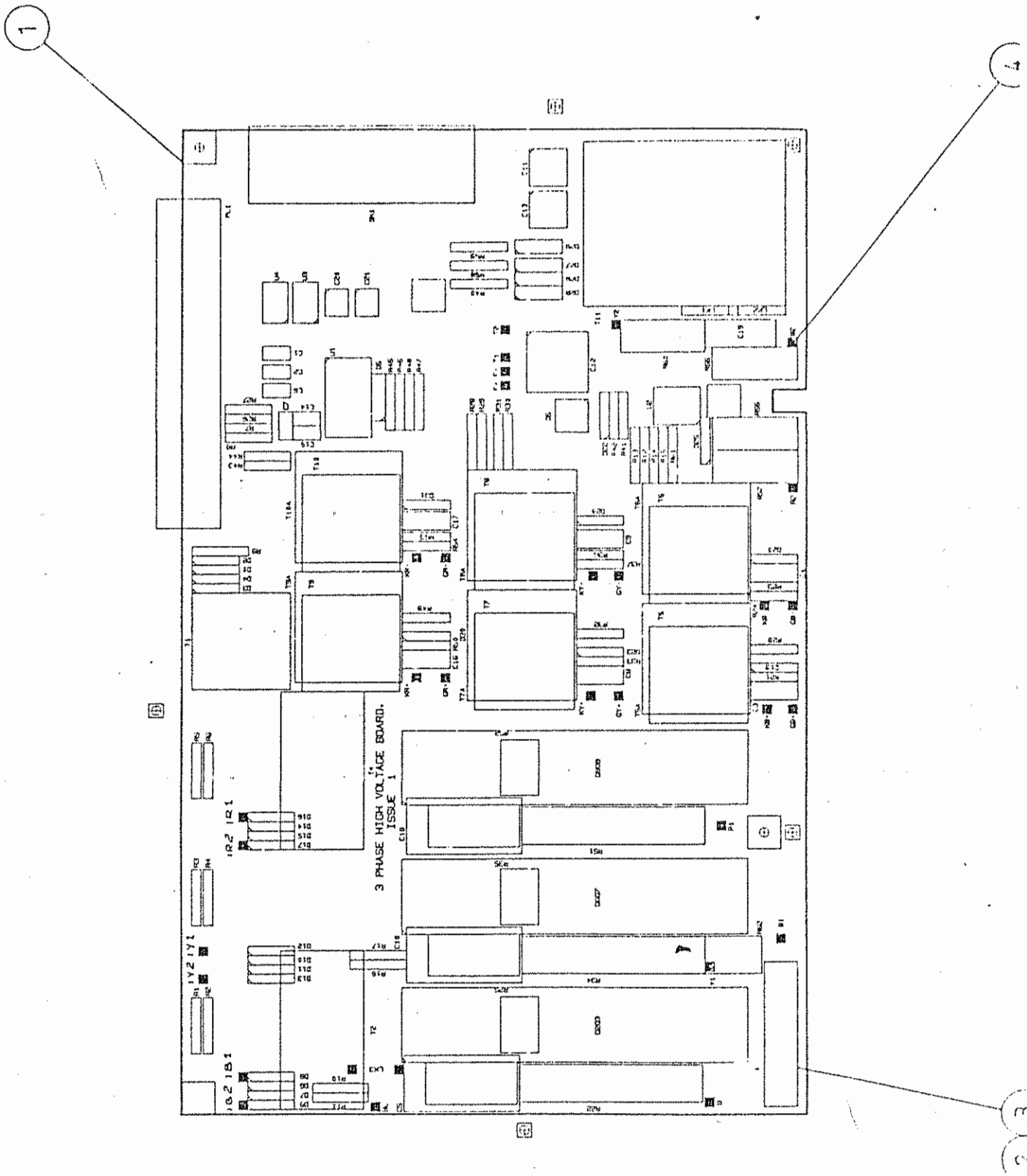
4 iii. Ancillary Circuits

d. Inhibit

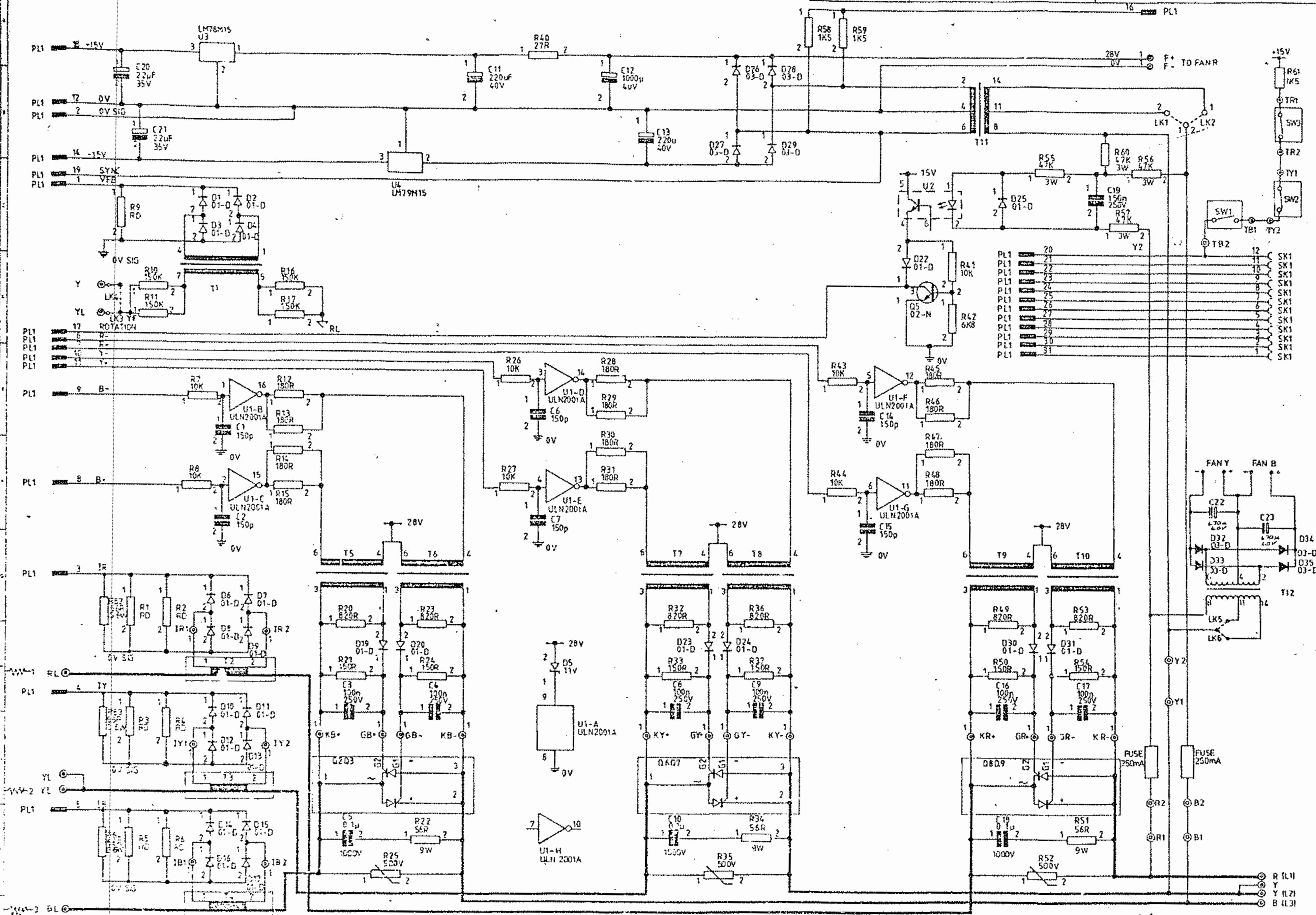
There are three ways that will cause the red inhibit LED to light. The first is if a signal between +5V and +30V is applied to the external inhibit input, terminal 11 on the 12 way small signal terminal. This will turn on TR3 and cause IC24.10 to go high. This will turn on TR2. The second way is if the over temperature trip goes open circuit. This is described under the section on circuit protection.

The third way is if the chop off feature is selected. TR2 is then driven via SW16 and D29. This occurs when the stack is quenched by an over-current condition. In this mode the stack is inhibited at switch on until a reset signal is applied to terminal 7 on the 12-way small signal terminal block. See under Limit modes for more information on the chop off feature.


DO NOT SCALE
THIRD ANGLE PROJECTION
GENERAL DRAWING PRACTICE TO BS 308/BS 3939
TO FAN
CURRENT | R1 R3 R5 | R2 R4 R6
25A | 470R | 2K7
50A | 200R | –
75A | 150R | 1K2
100A | 200R | 200R
150A | 150R | 200R
VOLTS | R9 | LK1 | LK2
220V | 1K5
240V | 1K5
380V | 1K
415V | 1K
440V | 1K
460V | 1K
480V | 1K
500V | 1K
NOTE 1
LOAD | LK3 | LK4
3 WIRE
4 WIRE
6 WIRE
NOTE 2
NOTE 1
TRANSFORMER T11
FOR 220/240 FIT C0021818
FOR 380-500 FIT C0021078
NOTE 2
LK3 IS 1/2" LINK
LK4 IS 4WIRE
MATERIAL
FINISH
414
SCALE
EUROTHERM
TITLE
3 PHASE HIGH VOLTAGE
CIRCUIT DIAGRAM
AI 021875 F 001
AI 021074
RE-NUMBERED


3 PHASE HIGH VOLTAGE BOARD.
ISSUE 1

DO NOT SCALE	THIRD ANGLE PROJECTION	GENERAL DRAWING PRACTICE TO BS 308/BS 3939



PL1
+15V
0V
0V SIG
-15V
SYNC
VFB
ROTATION
LM78M15
U3
LM79M15
U4
C20 22uF 35V
C21 22uF 35V
C11 220uF 40V
C12 1000μ 40V
C13 220u 40V
R40 27R
R58 1K5
R59 1K5
D26 03-D
D28 03-D
D27 03-D
D29 03-D
28V
F+ F- TO FAN R
T11
LK1
LK2
+15V
R61 1K5
TR1
SW3
TR2
TY1
SW2
SW1
TB1
TY2
TB2
R55 47K 3W
R60 47K 3W
R56 47K 3W
R57 47K 3W
C19 150n 250V
D25 01-D
U2
Q5 02-N
D22 01-D
R41 10K
R42 6K8
SK1
R9 RD
D1 01-D
D2 01-D
D3 01-D
D4 01-D
T1
R10 150K
R11 150K
R16 150K
R17 150K
LK3
RL
R7 10K
R8 10K
U1-B ULN2001A
U1-C ULN2001A
U1-D ULN2001A
U1-E ULN2001A
U1-F ULN2001A
U1-G ULN2001A
U1-H ULN 2001A
U1-A ULN2001A
C1 150p
C2 150p
C6 150p
C7 150p
C14 150p
C15 150p
R12 180R
R13 180R
R14 180R
R15 180R
R26 10K
R27 10K
R28 180R
R29 180R
R30 180R
R31 180R
R43 10K
R44 10K
R45 180R
R46 180R
R47 180R
R48 180R
T5
T6
T7
T8
T9
T10
D5 11V
FAN Y
FAN B
C22 470u 40V
C23 470u 40V
D32 03-D
D33 03-D
D34 03-D
D35 03-D
T12
LK5
LK6
R20 820R
R23 820R
R21 150R
R24 150R
D19 01-D
D20 01-D
C3 100n 250V
C4 100n 250V
KB+
GB+
GB-
KB-
Q2D3
C5 0.1μ 1000V
R22 56R 9W
R25 500V
R32 820R
R36 820R
R33 150R
R37 150R
D23 01-D
D24 01-D
C6 100n 250V
C9 100n 250V
KY+
GY+
GY-
KY-
Q4Q7
C10 0.1μ 1000V
R34 56R 9W
R35 500V
R49 820R
R53 820R
R50 150R
R54 150R
D30 01-D
D31 01-D
C16 100n 250V
C17 100n 250V
KR+
GR+
GR-
KR-
Q8Q9
C18 0.1μ 1000V
R51 56R 9W
R52 500V
FUSE 250mA
R1 R2 B1 B2 Y1 Y2
R1 RD
R2 RD
R3 RD
R4 RD
R5 RD
R6 RC
D6 01-D
D7 01-D
D8 01-D
D9 01-D
D10 01-D
D11 01-D
D12 01-D
D13 01-D
D14 01-D
D15 01-D
D16 01-D
D17 01-D
T2
T3
IR1
IR2
IY1
IY2
IB1
IB2
RL
YL
BL
R (L1)
Y
Y (L2)
B (L3)

CURRENT	175A	225A	325A	500A
R1 R3 R5	—	220R	2K2	56R 0.6W
R2 R4 R6	—	—	68R 0.6W	56R 0.6W

VOLTS	220V/240V	380V/415V	440/460/480/500V
R9	1K5	1K	1K
LK1&5		✓	
LK2&6	✓		✓
T11	[illegible]	[illegible]	[illegible]

LOAD	3 WIRE	4 WIRE	6 WIRE
LK3	✓	✓	
LK4			✓

ISS	ECN & DATE	DRN	CKD	DES APPR	MAN APPR
A	13/4/84				
B	4.97	SC			
1					

MATERIAL

FINISH

TOLERANCES UNLESS OTHERWISE STATED
DIMNS IN MM APPLY OVER FINISH
(EXCEPT FOR PAINT AND LACQUER)

ASSEMBLED ON 415

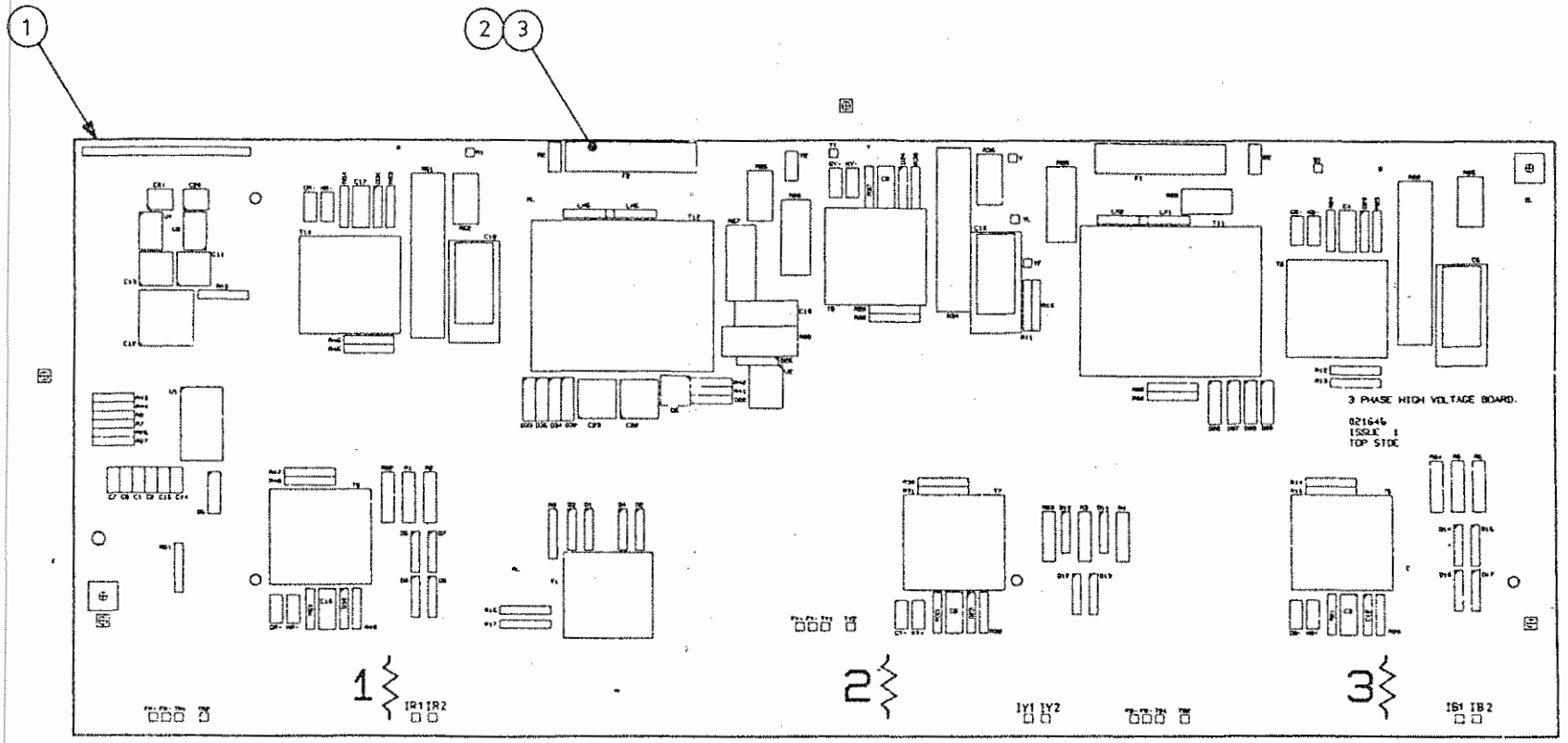
SCALE

EUROTHERM

TITLE
3 PHASE HIGH VOLTAGE BRD.
CIRCUIT DIAGRAM

DRAWING NUMBER A1 02164-5 F

SHT 1 OF 1 SHTS


1
2
3
3 PHASE HIGH VOLTAGE BOARD.
021646
ISSUE 1
TOP SIDE
1
IR1 IR2
2
IY1 IY2
3
IB1 IB2

THREE PHASE STACK CIRCUIT FUNCTIONALITY

4 iv. Control Circuits

a. Input Conditioning

The demand input signal to the unit is on terminal 1 (signal ref.) and terminal 2 (positive) on the 12-way small signal terminal. This signal can be seen on diagnostic point 4. Switches 1 to 4 are used to select the required input conditioning to normalise the output on IC1.8 to -5V. SW1 determines the span of the input, SW2 provides the offset and SW3 and SW4 convert mA signals to volts.

Input switches 1 to 4 are used to select the required input type. The following table indicates the various switch configurations.

INPUT	SW1	SW2	SW3	SW4
0-5V	0	0	0	0
1-5V	0	1	0	0
0-10V	1	0	0	0
0-5mA	0	0	1	0
0-10mA	1	0	1	0
0-20mA	0	0	1	1
4-20mA	0	1	1	1

In the table: 0 = switch open
1 = switch closed

There is a manual input on termial 3, also referenced to terminal 1, which is summed with the demand input. The scaling of this input is affected by the settings of SW1 and SW2.

Manual Input	SW1	SW2
0.5-5.5V	0	0
0.5-10.5V	1	0
1.3-6.3V	0	1
1.3-11.3V	1	1

This scaling is for Voltage inputs with demand input disconnected.

Manual Input	SW1	SW2
0-5V	0	0
0-10V	1	0
1.3-6.3V	0	1
1.3-11.3V	1	1

This scaling is for mA inputs or with demand input grounded.

4 iv. Control Circuits

b. Control Signal

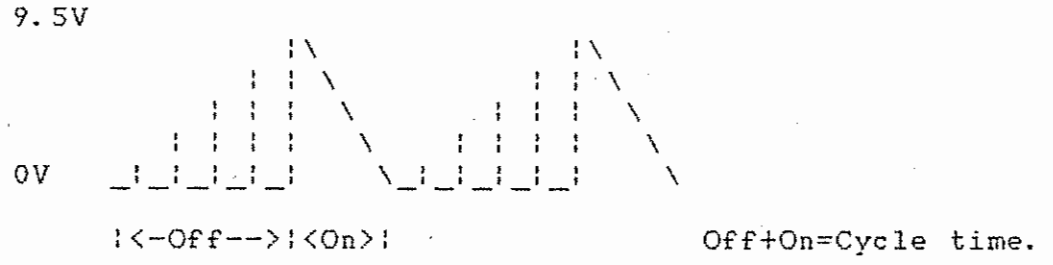
The buffered input signal is subtracted from the feedback signal at IC2.6 and the difference, or error value is intergrated by C8 or C8 plus C94. C8 on its own gives a integral time of 100mS. C8 and C94 will give an integral time of 2 secs.

This gives a 0-10V signal at IC2.7 which is inverted to give the 10-0V phase angle control signal at IC2.1. This signal can be seen on diagnostic point 12. The phase angle signal has a voltage swing of about +10.5V to -2V and has a dynamic range of approximately +9.3V at the start of conduction to +0.5V for full conduction.

4 iv. Control Circuits

c. Cycling Stage

The signal from IC2.7 is also fed to IC2.9. This op-amp acts as a hysteretic switch. Transistor TR1 is fed from the full wave rectified signal at IC5.7. This transistor therefore inhibits the signal from IC5.7 unless the supply waveform between line2 and line3 is around the zero point. When IC2.8 goes low (stack now fired) TR1 is held off by R48. IC2.8 will now remain low until signal from IC2.7 falls below the threshold level on IC2.10.



Waveform on collector of TR1.

The output on IC2.8 will be a rectangular waveform. The ratio of the ON and OFF times is determined by the buffered input signal and the feedback signal. The period (ON + OFF time) is controlled by SW12. With SW12 open the times are 400mS. + 400mS. at 50% power. With SW12 closed the times are 10S. + 10S. at 50% power.

The signal on IC2.8 is passed to a time delay circuit. The output of this circuit will overide the signal from IC2.7 when SW5 is closed. As this signal is switched from 0% to 100% cycling action will occur. With SW6 closed this will give a time delay of between 60mS. and 240mS. adjustable by RV3 (Soft Start pot).

This cycling mode with soft start and stop may be used in some applications that require current limit action or have transformer coupled loads where a reduction in interference due to continuous phase angle is required.

There will now be a phase angle section to the start and finish of each whole cycle period. This is the normal mode of operation where minimal supply disturbance is the criteria. If however D9 is fitted this will cause there to be a phase angle section only at the start of each on period with a hard stop. This may be required where interference needs to be kept to a minimum. This is the PS option.

Mode switches 5, 6, 12 are used to select the required firing mode. The following table indicates the various switch configuration.

MODE	SW5	SW6	SW12
Phase Angle 100mS. Ramp	0	X	0
Phase Angle 2 Sec. Ramp	0	X	1
Fast Cycle	1	0	0
Fast Cycle Soft Start	1	1	0
Slow Cycle	1	0	1
Slow Cycle Soft Start	1	1	1

In the table: 0 = switch open
1 = switch closed
X = don't care

4 iv. Control Circuits

d. Feedback

There are three possible feedback modes. These are V squared, V x I or I squared. The default feedback mode is V squared. In this mode a single load voltage signal is used. This signal is taken from across two of the load terminals for three and four wire loads. In the case of six wire loads, as one end of the loads are returned to a line, the load volts feedback is taken from one of the load line pairs. This change is accomplished by link3 and link4 on the High Voltage board which moves one end of the load volts signal isolating transformer T1 from the load to the line connection.

The voltage signal is converted to a current by R10,R11,R16 and R17 so that T1 is acting as a current transformer with about 24V on its primary when the stack is in full conduction. This current is converted back to a voltage, after rectification, by R9 on the High Voltage board in parallel with R86 on the Control board. The value of these two resistors range the stack for load volts according to the following table:

VOLTAGE	R9	R86
220V	1K5	15K
240V	1K5	6K2
380V	1K	2K4
415V	1K	1K8
440V	1K	1K5
460V	1K	1K3
480V	1K	1K2
500V	1K	1K1

All resistors are CA003... type. (0.5%, 50ppm)

The voltage developed across these resistors is the voltage feedback signal which can be seen on diagnostic point 20. With both SW7 and SW8 connected to the voltage feedback signal the multiplier IC7 will see this signal on both its inputs and therefore multiply this signal by itself to produce a V squared feedback signal at the multiplier output IC4.1. This signal can be seen on diagnostic point 9. It can be scaled by RV4 (Power pot) by +/-20% this is equivalent to a +/-10% change in load voltage.

In I squared feedback mode all three stack currents are monitored. The load bus bars each pass through a current transformer T2,T3 and T4. These CT's scale the load current by 2000:1 and after rectification will produce a 5V signal equivalent to max rms stack current across burden resistors R1 to R6 for 414 and R1 to R6 plus R62 to R64 for 415. The values of R1 to R6 range the maximum stack current according to the following table:

	CURRENT	R1=R3=R5	R2=R4=R6
414	25A	470R	2K7
	50A	200R	-
	75A	150R	1K2
	100A	200R	200R
	150A	150R	120R
415	175A	-	-
	225A	220R	-
	330A	2K2	68R @0.6W
	500A	56R @0.6W	68R @0.6W

The voltages developed across these resistors are the three current feedback signals IR, IY and IB. These three signals are summed at IC4.14. This signal can be scaled by RV5 which has a 5 to 1 range for load currents less than maximum. RV5 is factory set at the maximum current value. RV5 alters the I squared or VxI feedback signals. It does not affect the current limit signals.

The signal from IC14.14 is inverted at IC4.8 to give the summed current feedback signal. This signal is available at diagnostic point 11. As with the voltage feedback if both SW7 and SW8 are connected to the summed current feedback signal then the multiplier IC7 will produce the current squared feedback signal at IC4.1.

Of SW7 and SW8 if one is connected to the voltage feedback signal and one to the current feedback signal then the multiplier will produce the VxI feedback signal at IC4.1.

Feedback switches 7 and 8 are used to select the required feedback mode. The following table indicates the various switch configurations.

FEEDBACK	SW7	SW8
V Squared	1	1
V x I	1	2
or	2	1
I Squared	2	2

In the table: 1 = change over link position nearest right hand side of board.
2 = change over link position nearest left hand side of board.

Board to be viewed as per configuration diagram.

4 iv. Control Circuits

e. Limit Modes

There are a number of limiting conditions which can be imposed upon the operation of the stack according to the application requirements. Where limit control is affected by RV2, the LIMIT potentiometer on the front panel, then according to the selection of SW9 this control can be from the internal 10V reference or from an external signal. If the external signal is selected then RV2 will be in cascade with it. This will allow a scaling effect on the external limit signal.

i. Current threshold.
The various limit modes are selected with SW13 to SW17. In most modes SW17 will be closed. This switch engages the three current limit feedback signals from IC3.14, .1 and .7. The three current feedback signals IR, IY and IB go to a two breakpoint squaring circuit around TR5, TR6 and TR7 respectively. If we take the circuit on the red (L1) phase then the squaring circuit will produce a current at IC3.13.

This current is backed of by a threshold current through R55. The sum of these two currents is intergrated by C14 and will drive the output on IC3.14 low if the feedback current exceeds the threshold current. The level of this threshold can be varied by RV2 if SW13 is closed. The voltage on the wiper of RV2 is inverted at IC1.14 to give a 0V to -5.5V signal equivalent to 0 to max line current setting. This can be seen at diagnostic point 2.

The three current limit feedback signals are proportional to I squared as this gives the correct protection against overheating and are OR'd together by diodes D12, D15 and D18 to give a lowest wins condition. The largest of the three currents will pull back the phase angle of all three lines. When a disable condition exists the output of the three integrators, along with the main loop integrator, are held low by the analogue switches of IC8.

ii. Demand threshold.
If SW13 is open and SW14 is closed then RV2 will control the maximum demand input. RV2 will set a level between 0V and -5.5V on the input IC3.10. The other input IC3.9 monitors the buffered (demand) input. If the demand input tries to exceed (more negative) the set threshold then IC3.8 will start to go positive and clamps the buffered (demand) input. As both the current limit threshold and demand limit threshold require RV2 for their setting these two options are mutually exclusive.

iii. V/I transfer.
SW15 selects the V/I transfer mode of operation. If the load impedance is greater than Vnominal/Inominal then control of the load will be undertaken by the main feedback loop. If the load impedance is less than this then the highest of the current limit loops will take control. The current limit setting is determined by the buffered (demand) input via SW15. As this signal will now overide the current threshold limit signal via SW13 these two modes are therefore mutually exclusive.

Although the mode is called V/I transfer the main loop need not be in V squared feedback. With V/I transfer, demand limit SW14 can also be selected. As the demand input determines the point of current limit, then demand limit will control the maximum demand or the maximum current in the load depending on the load impedance.

iv. Chop off.
The chop off feature is selected with SW16. As this feature works on current overloads the current limit must be disabled. This is done by opening SW17. The use of a demand limit, SW14, may be used if required.

The chop off circuit looks at the peak currents of the three thyristor pairs via diodes D33, D34 and D35. If one of these peaks exceed the level set at IC33.3 then the output at IC33.1 will go to 0V. This will pull the input of schmitt-nand IC24.12 low, and its output IC24.11 high. This output is diode OR'd via D29 with the inhibit signal. So this output going high will quench the stack.

As the stack has now quenched, the overload condition has therefore been removed. To prevent the stack from powering up immediately a time delay of approximately 0.25 seconds is introduced by R184 and C107.

When IC33.1 goes low and the stack quenches, a diode pump action occurs with D32 and C109. If a number, approximately four, succesive quenches occur then the voltage on C109 will be pumped below the level set at IC33.5 causing IC33.& to go high. The charge on C109 is reset by R194. IC33.7 going high causes the NOR output IC20.11 to go low. This is connected to analogue control gate IC32.5 which turns off causing IC32.4 to go high, this in turn latches the output of IC20.11 which holds IC24.11 high and the stack inhibited.

To release the stack a reset signal is applied to terminal 7 of the 12-way small signal terminal block. This turns TR9 on pulling IC20.13 low, IC20.11 will go high so turning on the analogue gate and holding the input low until the next overload. If TR9 is held on the stack will never latch out.

The size of the overload is dependant on the normal load current. If the unit is running at its maximum rms current at its maximum ambient, then no overload is permitted. Use of this feature therefore requires the stack to be sized in excess of the normal running current.

Limit switches 13, 14, and 15 are used to select the required limit control. Switches 16 and 17 relate to the Chop Off feature. The following table indicates the various switch configurations.

CONTROL	SW13	SW14	SW15	SW16	SW17
No Limit	0	0	0	0	1
Current Threshold	1	0	0	0	1
Power(demand) Threshold	0	1	0	0	1
Volt/Current Transfer	0	0	1	0	1
V/I Trans & Pwr Threshold	0	1	1	0	1
Chop Off	0	0	0	1	0
Chop Off & Pwr Threshold	0	1	0	1	0

In the table: 0 = switch open
1 = switch closed

Limit switch 9 is used to select the source of the limit setting. This can be internal via front panel pot P3, or from an external potentiometer or external signal via the signal terminal block.
The following table indicates the two switch positions:

SETTING	SW9
Internal	2
External	1

In the table: 1 = change over link position nearest right hand side of board.
2 = change over link position nearest left hand side of board.

Board to be viewed as per configuration diagram.

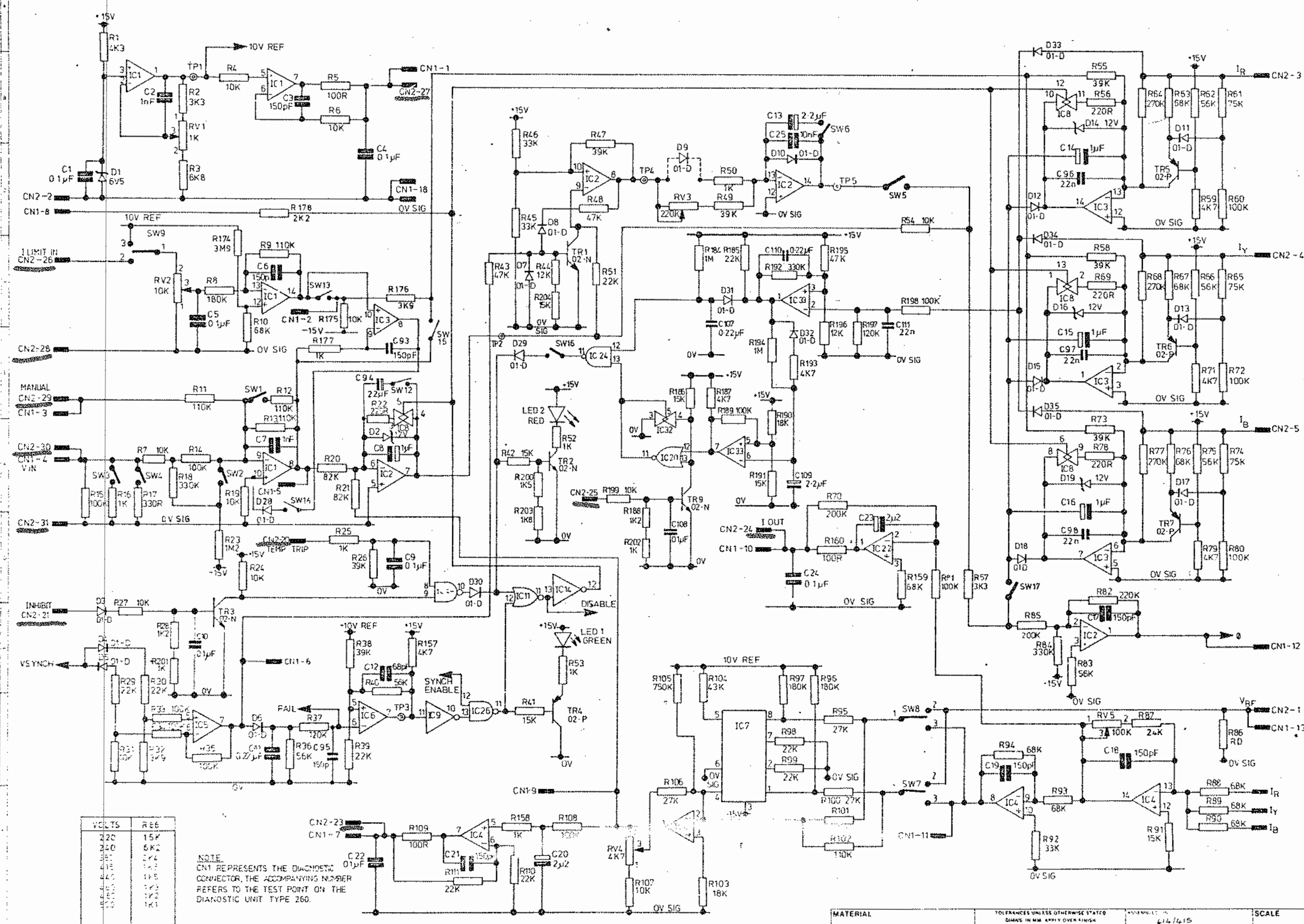
4 iv. Control Circuits

f. Monitored signals

There are two signals available on the 12 way small signal terminal. The first is available on terminal 8. This is the monitored load current signal. The signal is taken from IC4.14 where the three load currents had been summed. This signal is smoothed by C23 and buffered at IC22.1. The signal is scaled by RV5 to give 10.0V at the maximum rated current.

The second signal is available on terminal 9 and is the monitored feedback signal. The signal is taken from IC4.1 the feedback signal. It is smoothed by C20 and buffered at IC4.7. This signal is dependant on the feedback mode selected to give a V squared, I squared or VxI(power) signal. The signal is scaled by RV4 to give 8.2V at nominal voltage or NOMINAL current ratings.

DO NOT SCALE | THIRD ANGLE PROJECTION | GENERAL DRAWING PRACTICE TO BS 308/BS 3939



VOLTS	R66
220	15K
240	6K2
[illegible]	[illegible]
[illegible]	[illegible]
440	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]
[illegible]	[illegible]

NOTE
CN1 REPRESENTS THE DIAGNOSTIC CONNECTOR, THE ACCOMPANYING NUMBER REFERS TO THE TEST POINT ON THE DIANOSTIC UNIT TYPE 260.

MATERIAL

FINISH

TOLERANCES UNLESS OTHERWISE STATED
DIMNS IN MM APPLY OVER FINISH
(EXCEPT FOR PAINT AND LACQUER)

ASSEMBLY 414/415

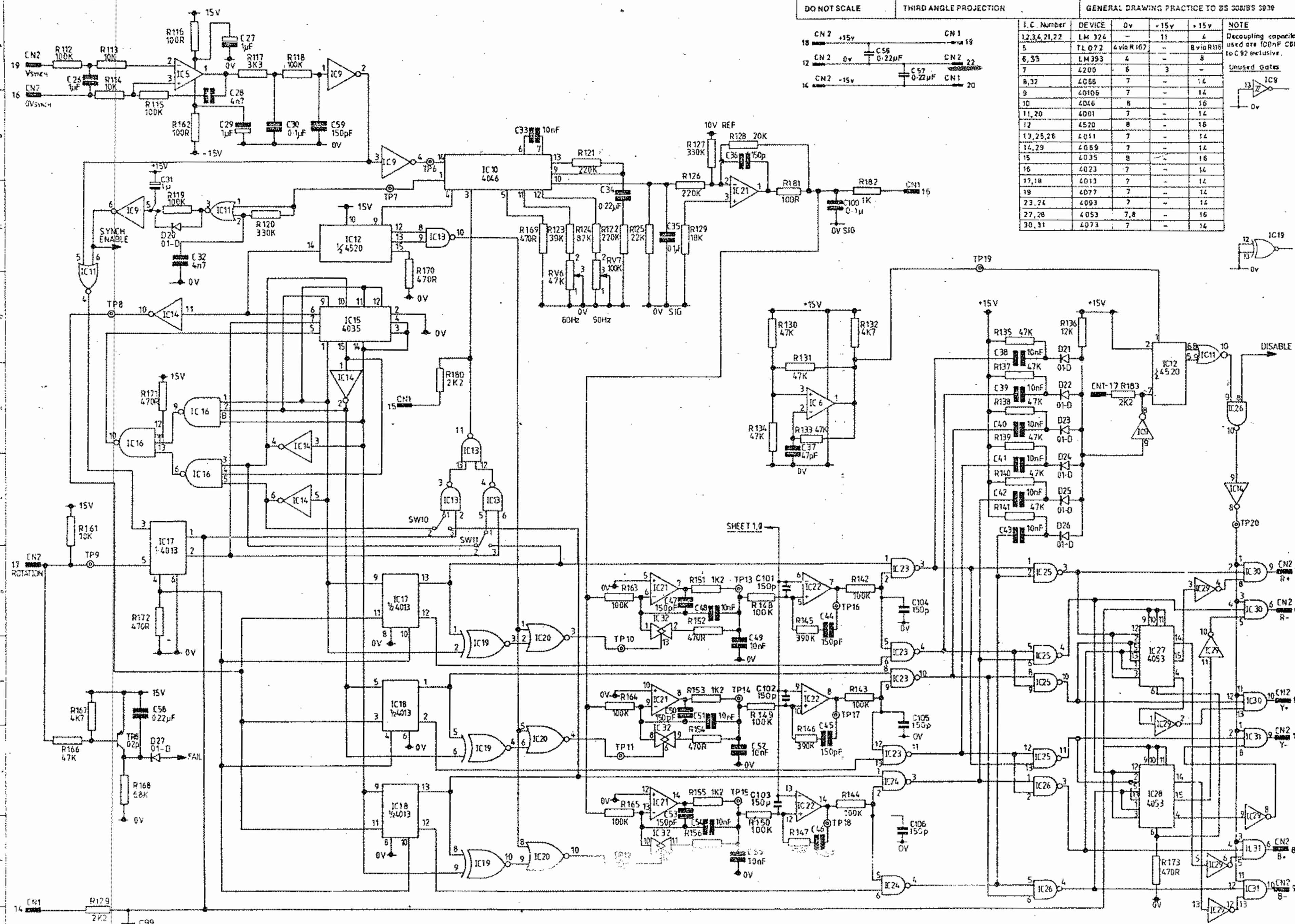
SCALE

EUROTHERM

TITLE
3 PHASE STACK CONTROL BOARD WITH CHOP-OFF CIRCUIT DIAGRAM

A1 022059 F001

DO NOT SCALE | THIRD ANGLE PROJECTION | GENERAL DRAWING PRACTICE TO BS 308/BS 3939



I.C. Number	DEVICE	0v	-15v	+15v
1,2,3,4,21,22	LM 324	–	11	4
5	TL 072	4 via R 167	–	8 via R116
6,33	LM 393	4	–	8
7	4200	6	3	–
8,32	4066	7	–	14
9	40106	7	–	14
10	4046	8	–	16
11,20	4001	7	–	14
12	4520	8	–	16
13,25,26	4011	7	–	14
14,29	4069	7	–	14
15	4035	8	–	16
16	4023	7	–	14
17,18	4013	7	–	14
19	4077	7	–	14
23,24	4093	7	–	14
27,28	4053	7,8	–	16
30,31	4073	7	–	14

NOTE
Decoupling capacitors used are 100nF C60 to C92 inclusive.

Unused Gates

MATERIAL

FINISH

TOLERANCES UNLESS OTHERWISE STATED

ASSEMBLY ON 414/415

SCALE

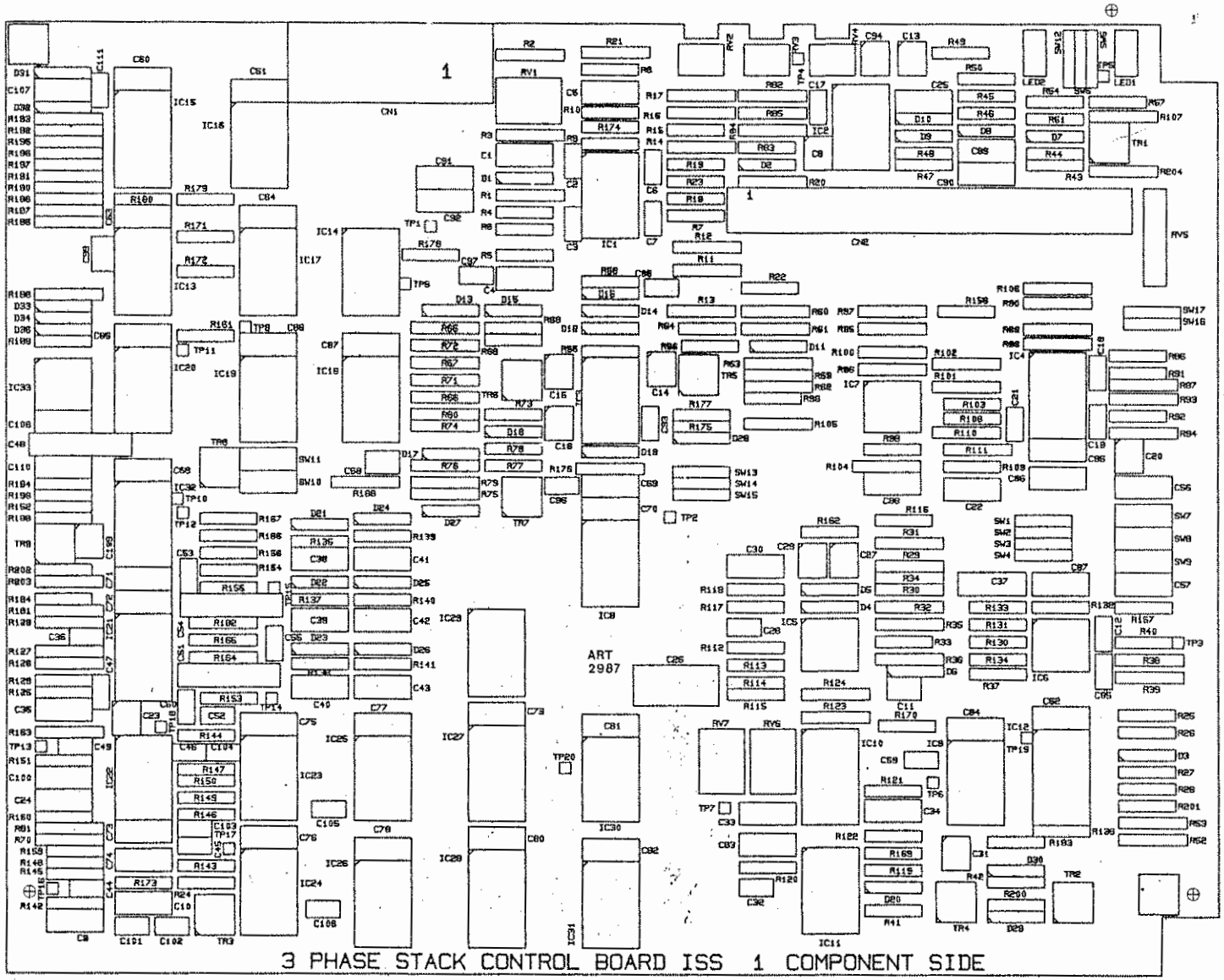
EUROTHERM

TITLE
3 PHASE STACK CONTROL BOARD WITH CHOP-OFF CIRCUIT DIAGRAM

DRAWING NUMBER AI 022059 F001

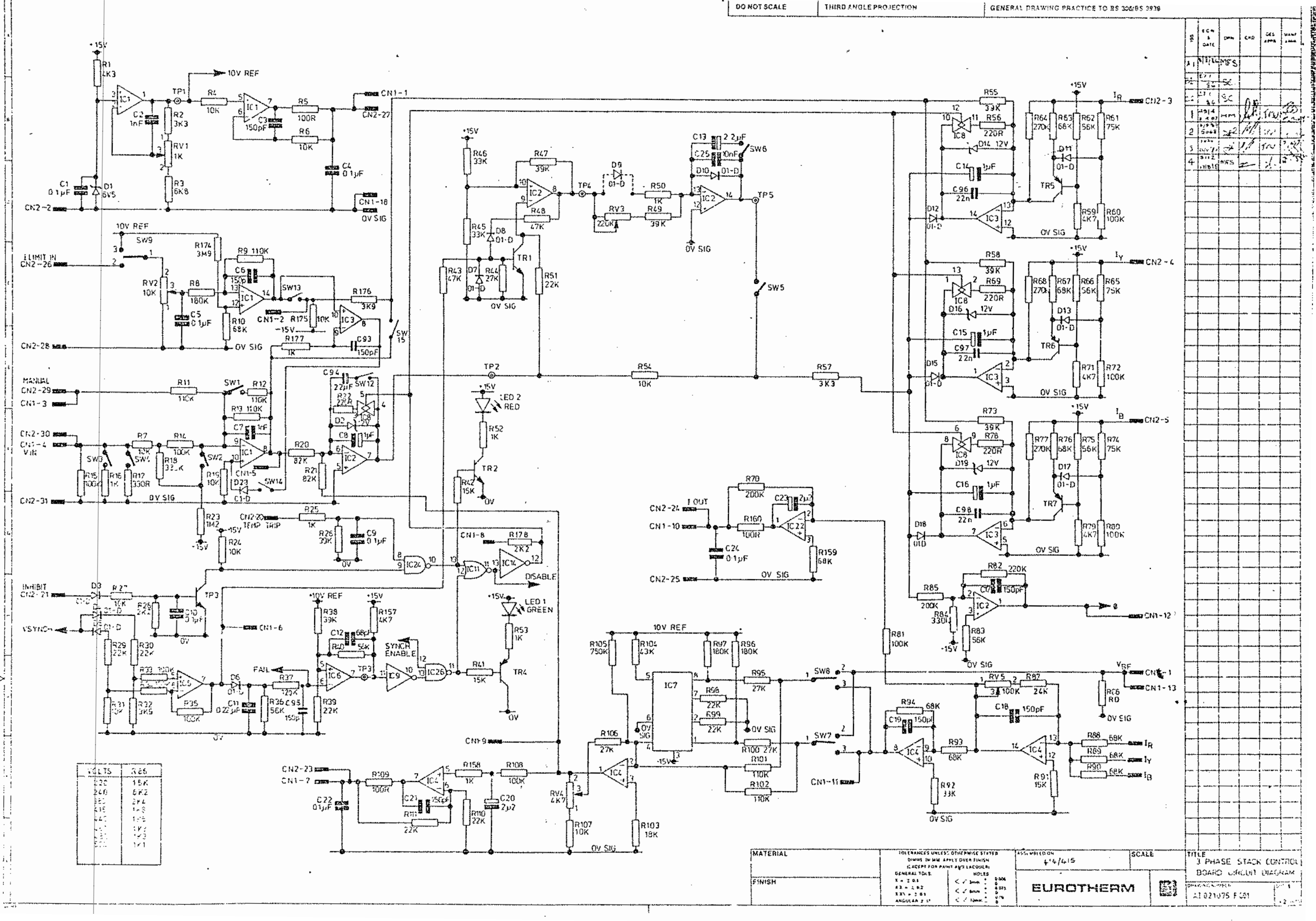
SH 2 OF 2

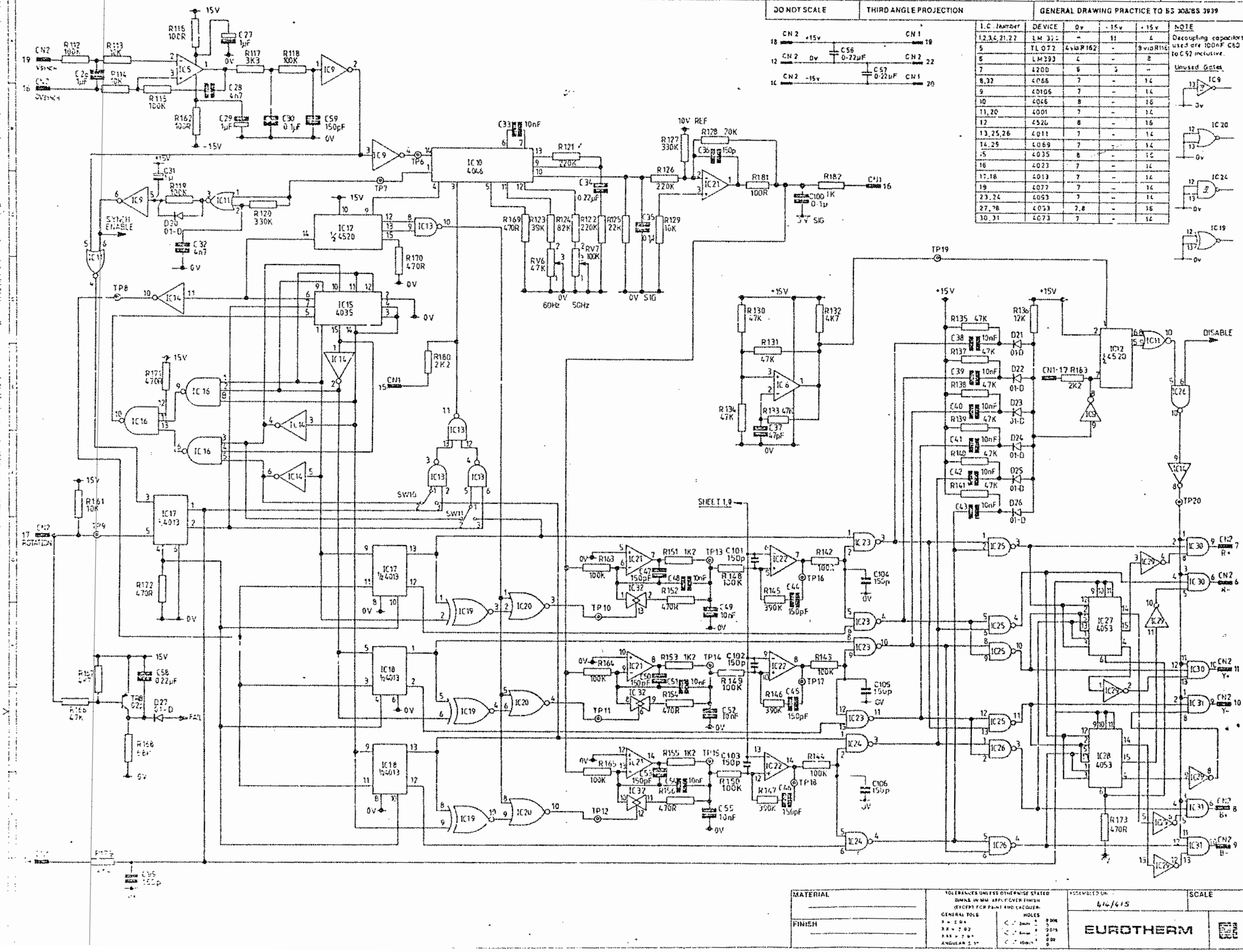
(0483) 502003



3 PHASE STACK CONTROL BOARD ISS 1 COMPONENT SIDE

EUROTHERM
3 PHASE CNTRL BD+CHOP-OFF
COMPONENT IDENT
(SEC MASTER)


DO NOT SCALE
THIRD ANGLE PROJECTION
GENERAL DRAWING PRACTICE TO BS 308/BS 3939
MATERIAL
FINISH
SCALE
EUROTHERM
TITLE
3 PHASE STACK CONTROL
BOARD CIRCUIT DIAGRAM
AI 021075 F C01



DO NOT SCALE

THIRD ANGLE PROJECTION

GENERAL DRAWING PRACTICE TO BS 308/BS 3939

I.C. Number	DEVICE	0v	-15v	+15v
12,34,21,22	LM 324	-	11	4
5	TL072	4 via R162	-	8 via R116
6	LM393	4	-	8
7	4200	6	3	-
8,32	4066	7	-	14
9	40106	7	-	14
10	4046	8	-	16
11,20	4001	7	-	14
12	4520	8	-	16
13,25,26	4011	7	-	14
14,29	4069	7	-	14
15	4035	8	-	16
16	4023	7	-	14
17,18	4013	7	-	14
19	4077	7	-	14
23,24	4093	7	-	14
27,28	4053	7,8	-	16
30,31	4073	7	-	14

NOTE
Decoupling capacitors used are 100nF C60 to C92 inclusive.

Unused Gates

MATERIAL

FINISH

TOLERANCES UNLESS OTHERWISE STATED

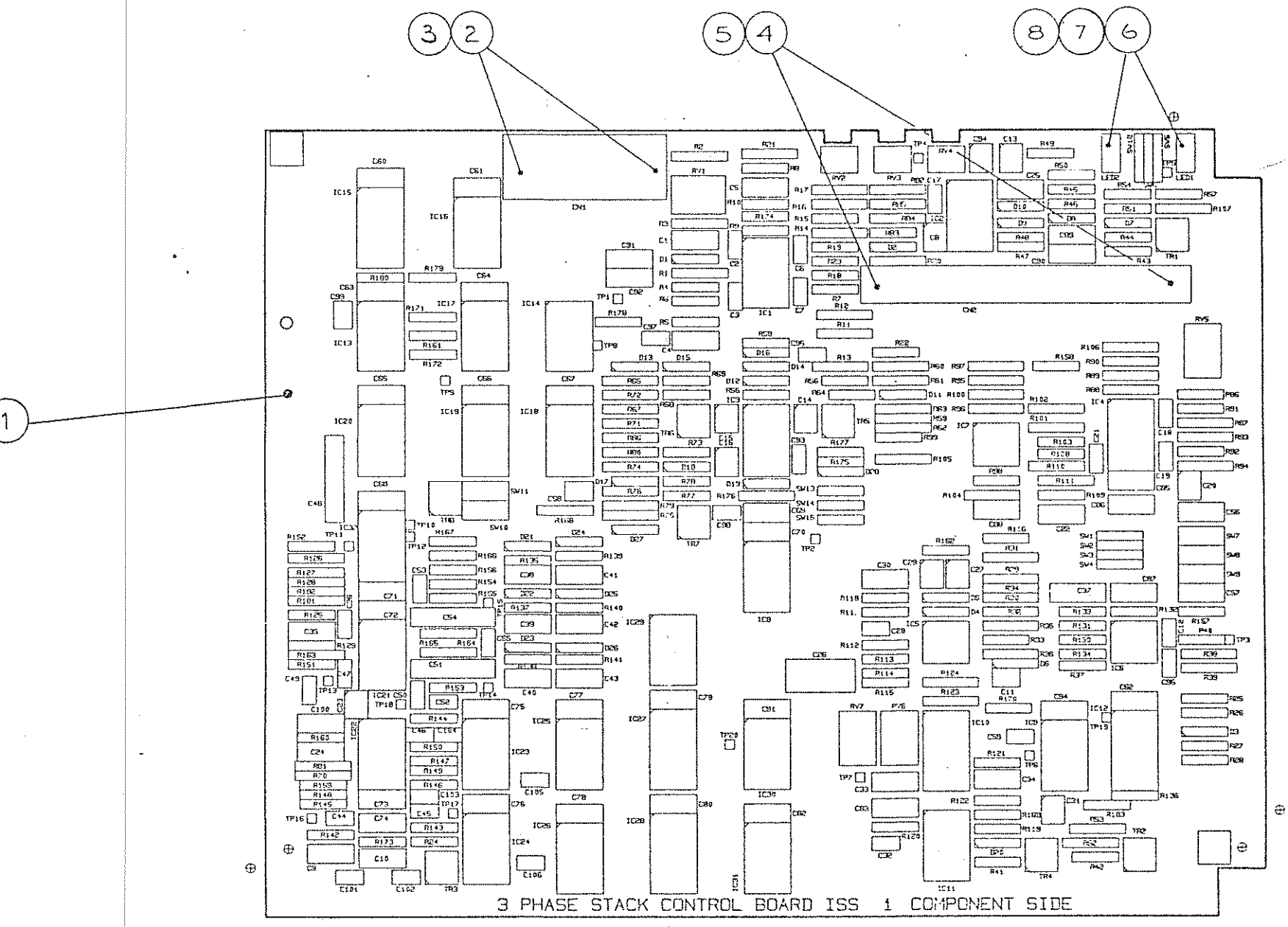
ASSEMBLED ON: 414/415

SCALE

EUROTHERM

TITLE
3 PHASE STACK CONTROL BOARD CIRCUIT DIAGRAM

AI 021075 F001


3
2
5
4
8
7
6
1
3 PHASE STACK CONTROL BOARD ISS 1 COMPONENT SIDE

5. DIAGNOSTIC POINTS

The unit has a 20 way diagnostic connector fitted to it behind the front panel door. This is for use with a 260 diagnostic unit. The diagnostic points are as follows:

No.		Title.	260 reading.
1.		+10V reference.	10V +/-30mV.
2.		Buffered limit input.	0V to -5.5V.
3.		Manual input.	0V to 5 or 10V.
4.		Setpoint input.	0V to 5 or 10V.
5.		Buffered setpoint.	0 to -5V.
6.	*	Mains sense 8Vpeak full wave.	5.3V.
7.		Buffered monitored feedback.	0 to 10V.
8.		Disable signal.	0V. (15V=Disable)
9.	*	Power feedback.	0 to 5V.
10.		Buffered monitored sum of currents.	0 to 10V.
11.	*	Summed current feedback voltage.	0 to 5V.
12.		Phase angle signal.	10 to 0V.
13	*	Voltage feedback.	0 to 5V.
14.		Rotation signal. Forward/Reverse	0V/15V.
15.	*	Phase lock loop feedback.	7.5V
16.		50/60Hz trim voltage.	-1V/-1.2V
17.	*	First pulse signal.	0V or 0.3V
18.		0V. signal.	0V.
19.		+15V. supply.	14.3V to 15.7V.
20.		-15V supply.	-14.3V to -15.7V.

* = Signal waveform is not dc, voltage level given is average reading on diagnostic meter.

6. SPARE PARTS

414 FUSE SELECTION

STACK RATING	FUSE				
	Brush	Dorman Smith	Ferraz	GEC	IR
25A	32ET 35FE	DSG 1000/30	6.6URS17/32	GSG 1000/30	E1000-30
50A	80ET 80FE	DSG 1000/70	6.6URS17/75 6.6URS17/80		E1000-75
75A	90EET	DSG 1000/85	6.6URT217/90	GSG 1000/85	EE1000-90
100A	120FEE	DSG 1000/110	6.6URT217/110	GSG 1000/110	
150A		DSG 1000/150	6.6URT217/160	GSG 1000/150	

415 FUSE SELECTION

STACK RATING	FUSE		
	Bussmann	Ferraz	Gould Shawmut
175A	170L4949	D 87012	A1-66S250TS
225A	170L5541	E 87013	A1-66S315TS
330A	170L5543	F 87014	A1-66S400TS
500A	170L5546	N 78005	A1-66S630TS

PARTS			PART NUMBERS
414 FUSES	25A	-	CS021876U001
	50A	-	CS021876U002
	75A	-	CS021876U003
	100A	-	CS021876U004
	150A	-	CS021876U005
415 FUSES	175A	-	CS021796U001
	225A	-	CS021796U002
	330A	-	CS021796U003
	500A	-	CS021796U004

414/415 CONTROL PCB	-	AH022059U002
414 HIGH VOLTAGE PCB	-	AH021875U002
415 HIGH VOLTAGE PCB	-	AH021645U002
380-500V MAINS TRANSFORMER	-	CO021078
220-240V MAINS TRANSFORMER	-	CO021818
PCB FUSE 250mA/660V	-	CH200251
MOV 500V	-	CK013407